

FIG. 5

FIG. 6

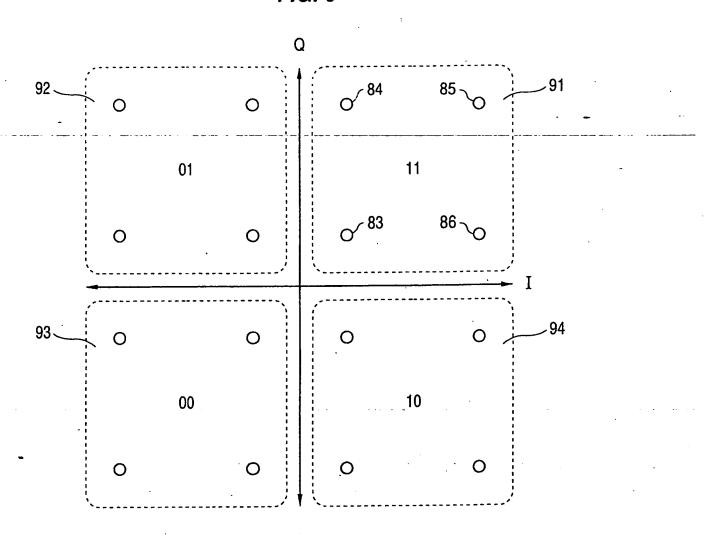


FIG. 7

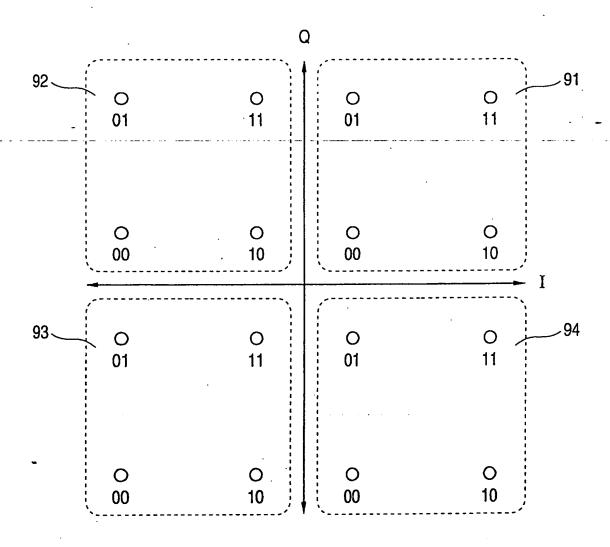
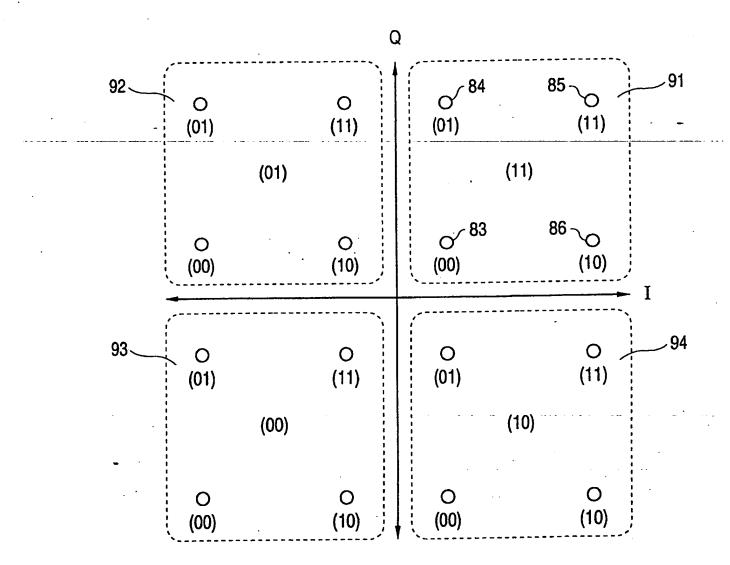


FIG. 8



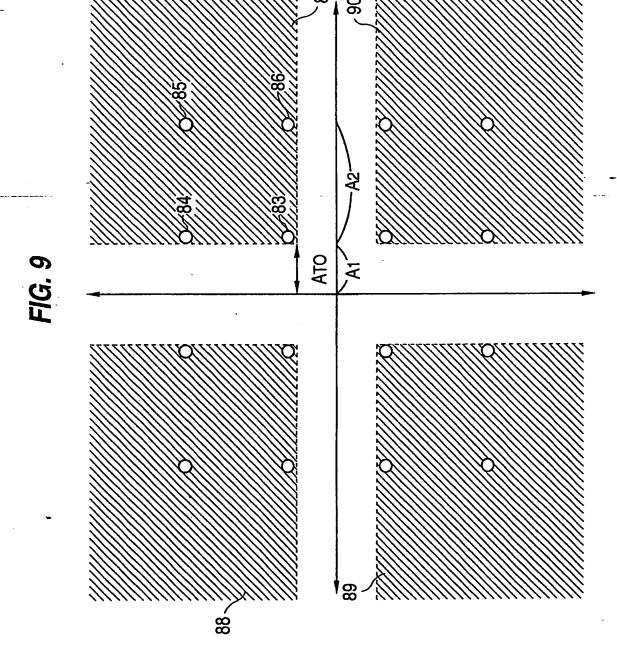
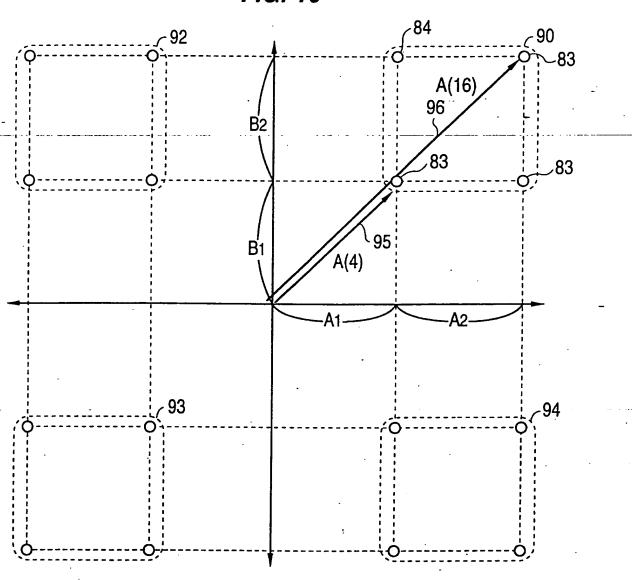


FIG. 10



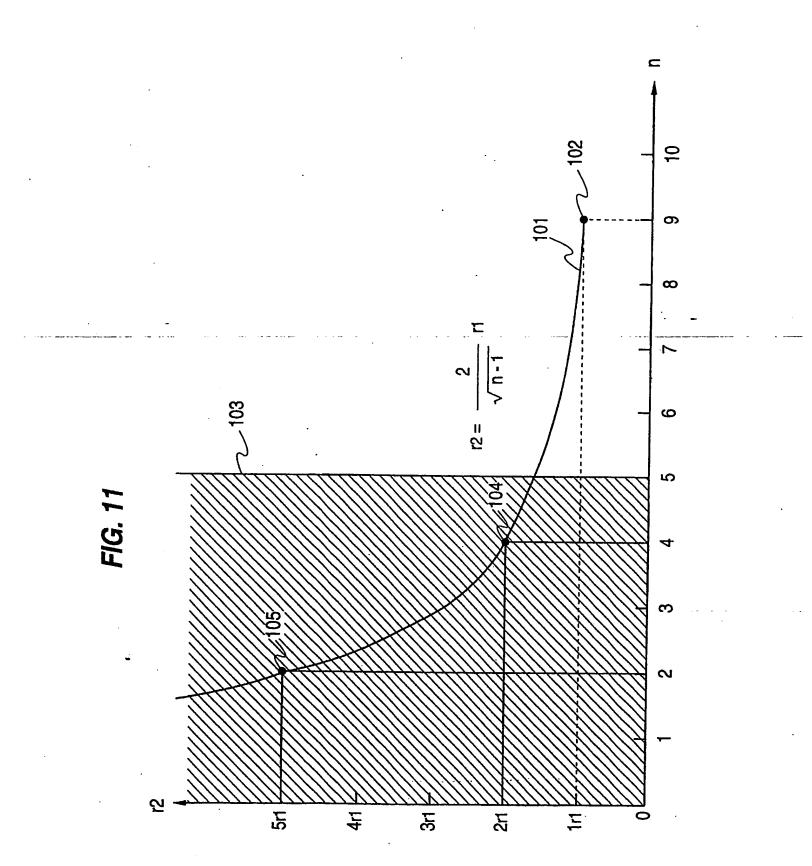
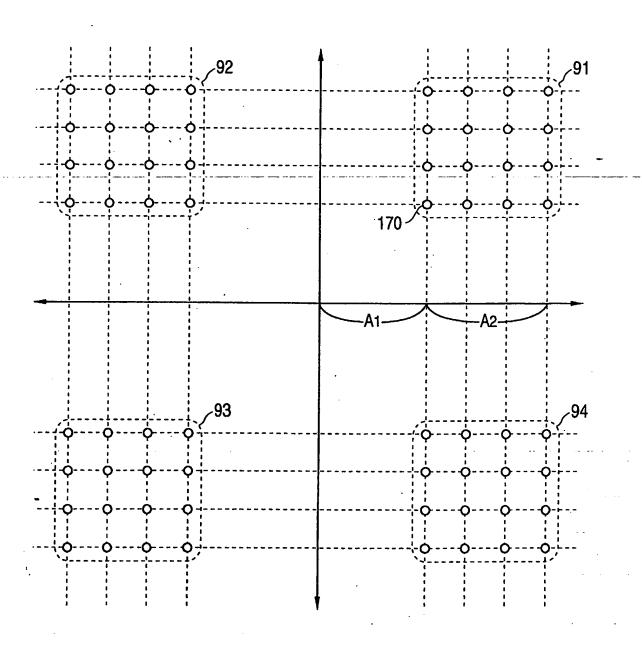


FIG. 12



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U.S. Patent

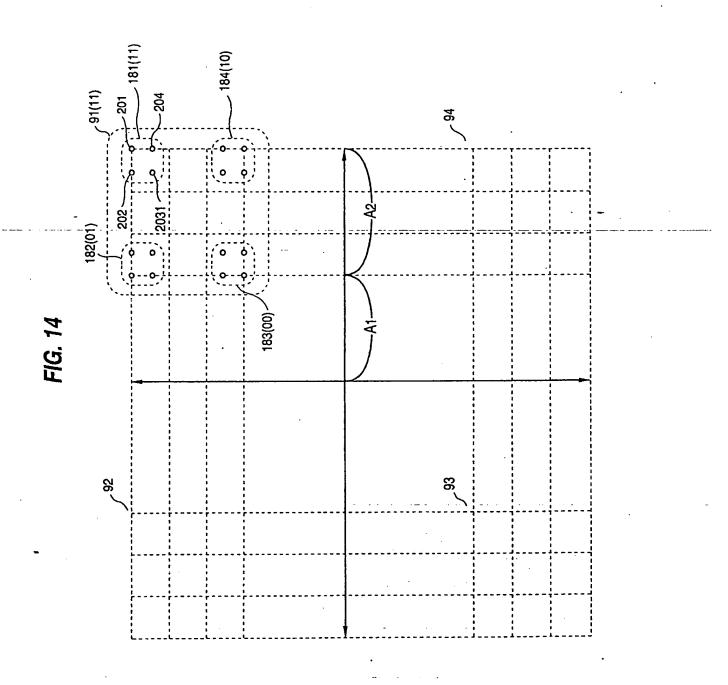
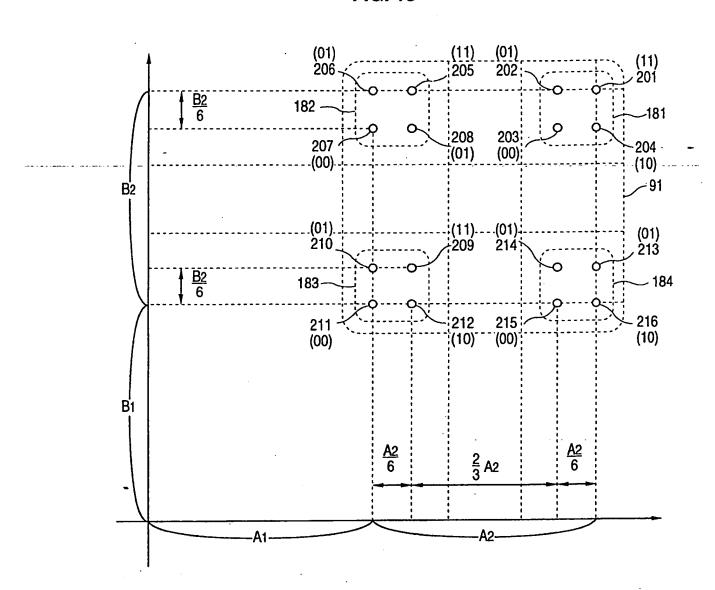
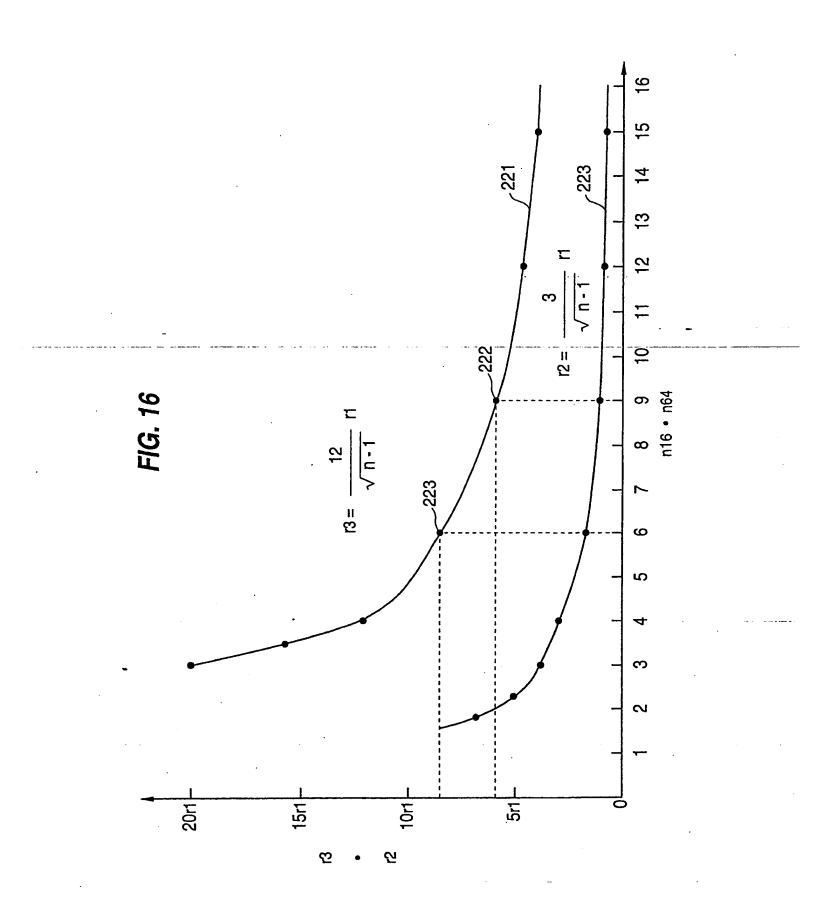


FIG. 15





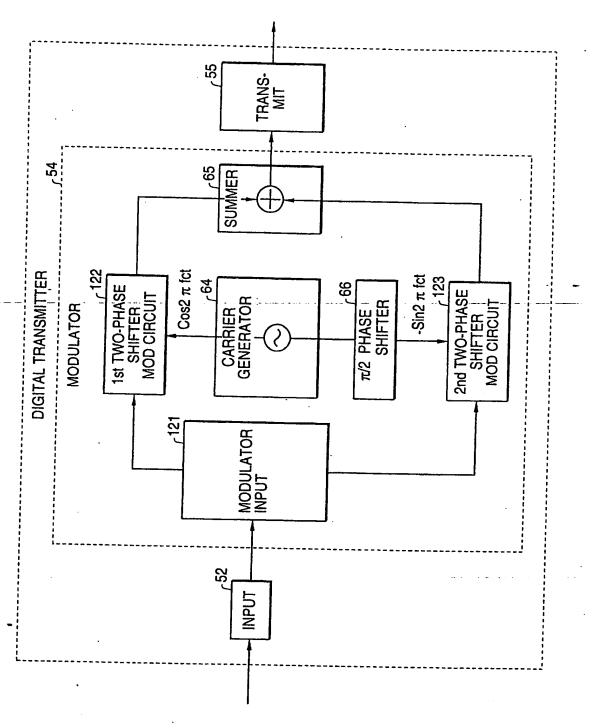
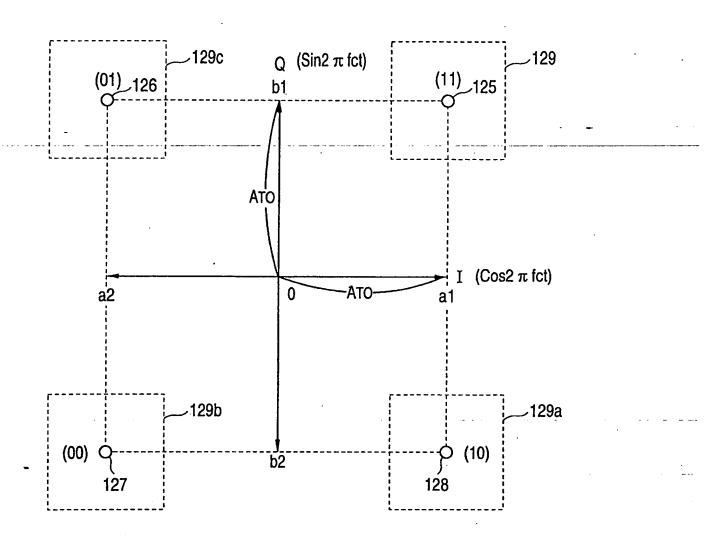


FIG. 18



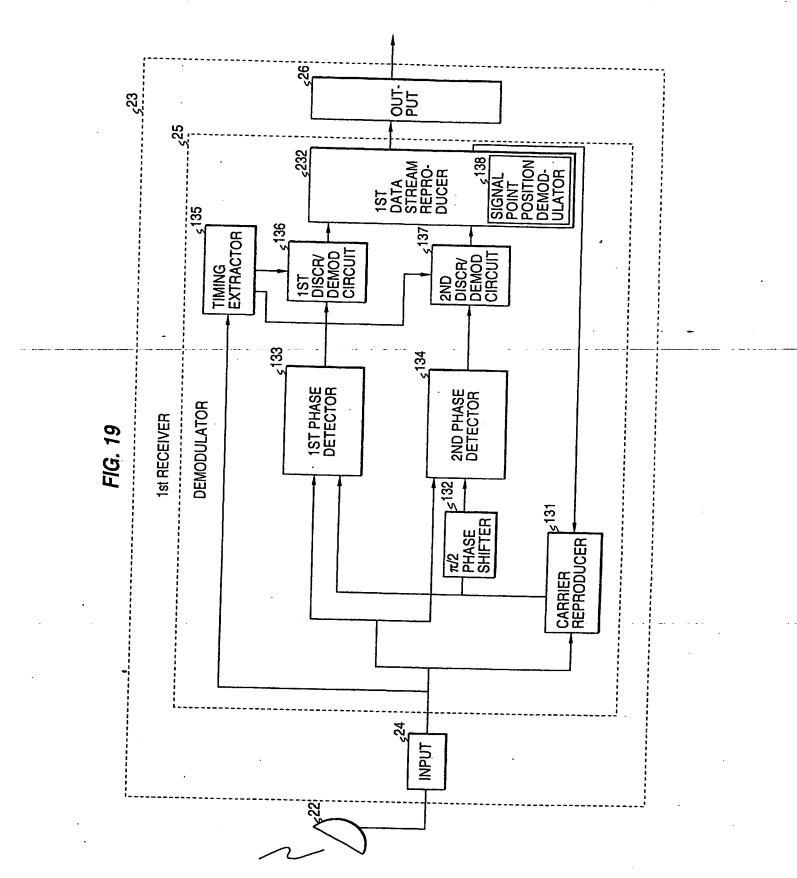
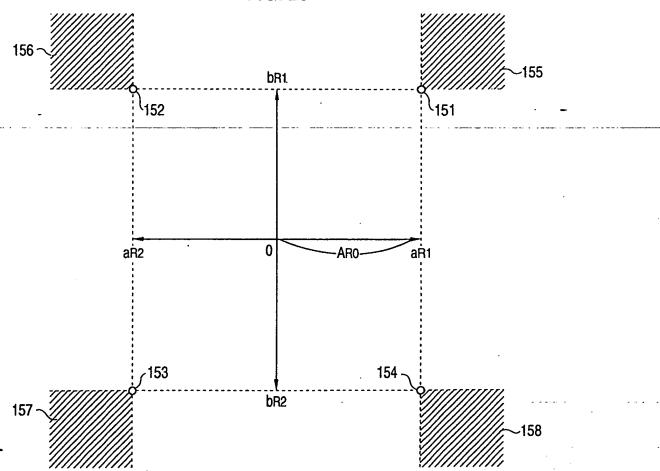


FIG. 20



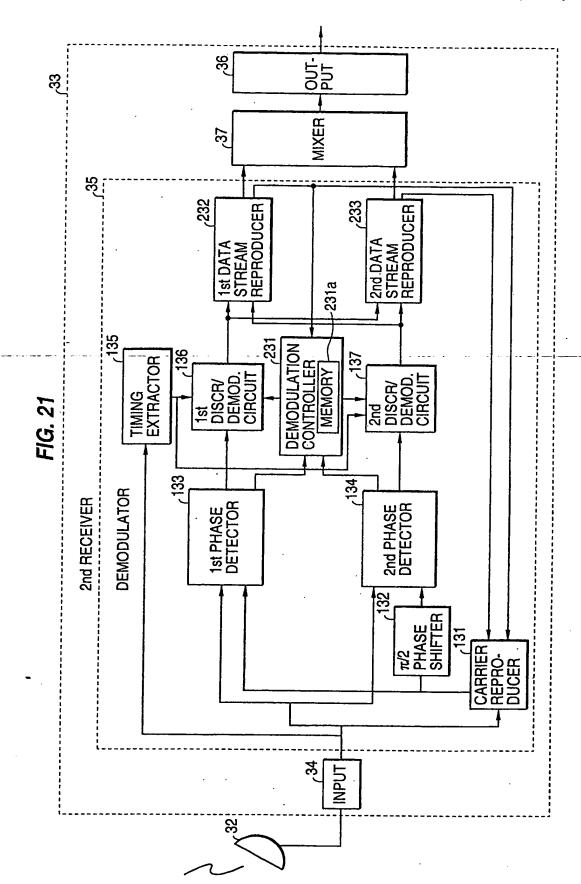
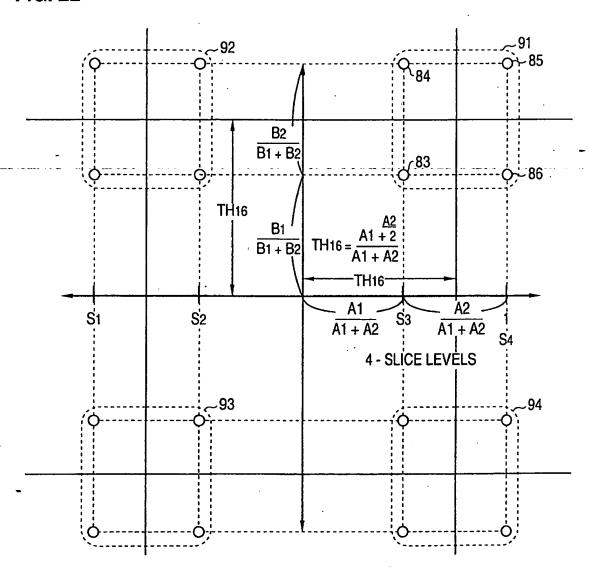


FIG. 22



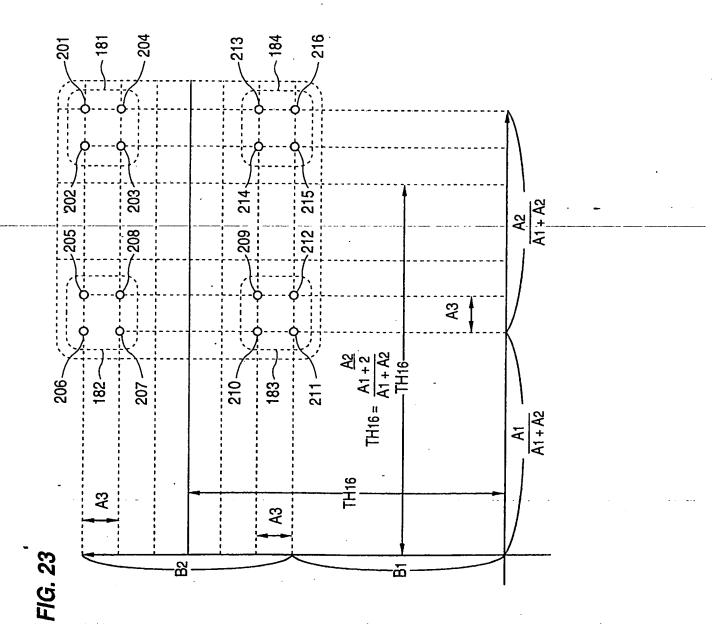
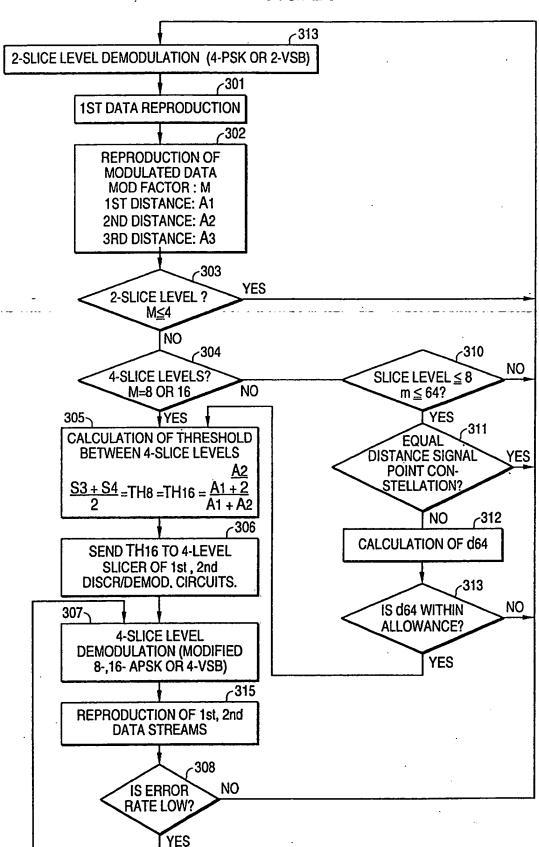
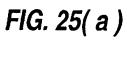


FIG. 24





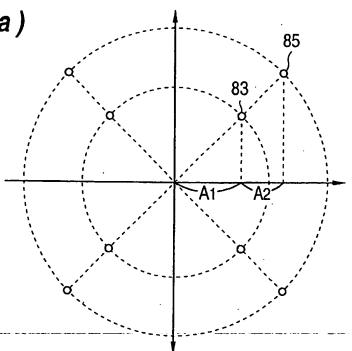
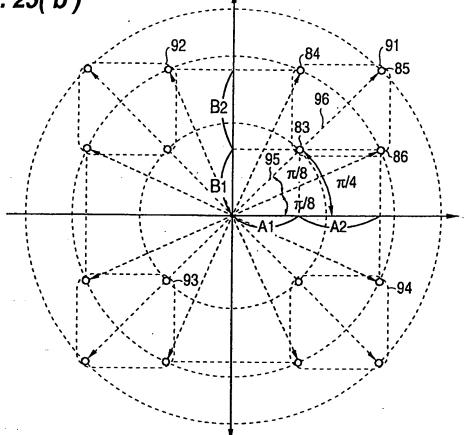


FIG. 25(b)



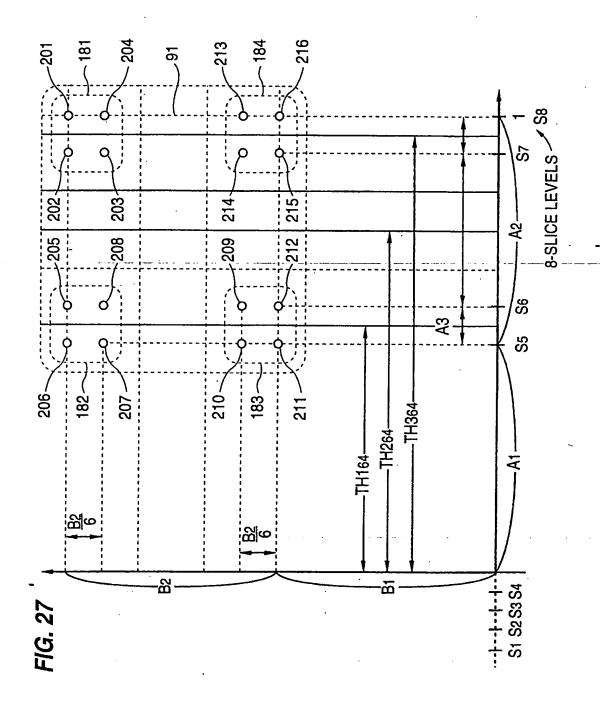
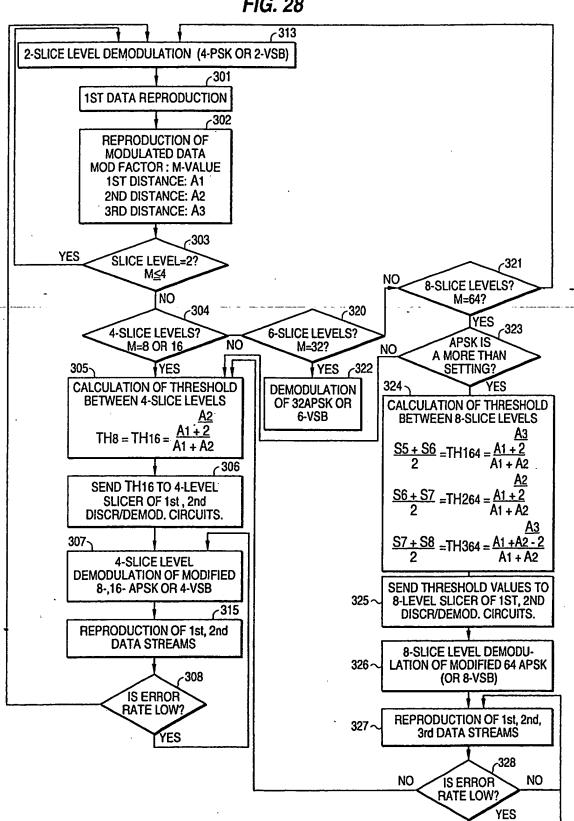
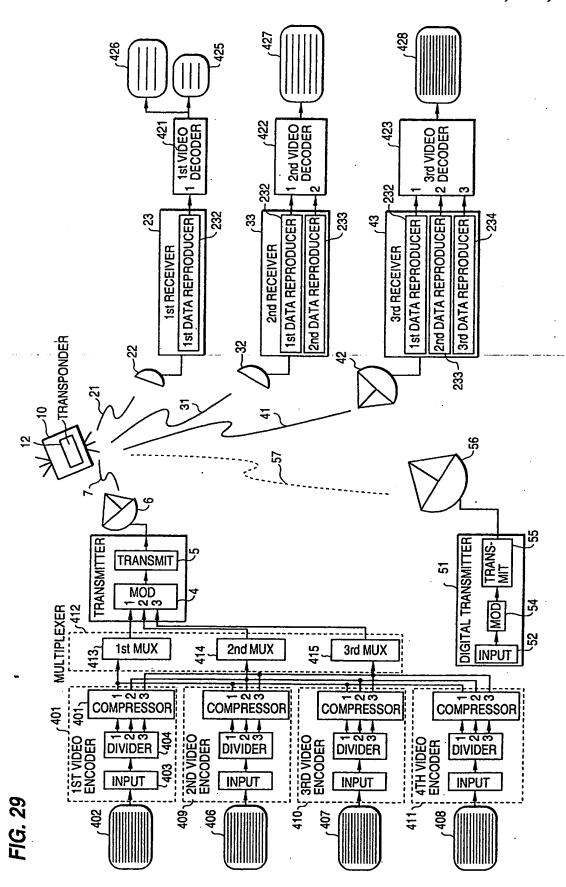
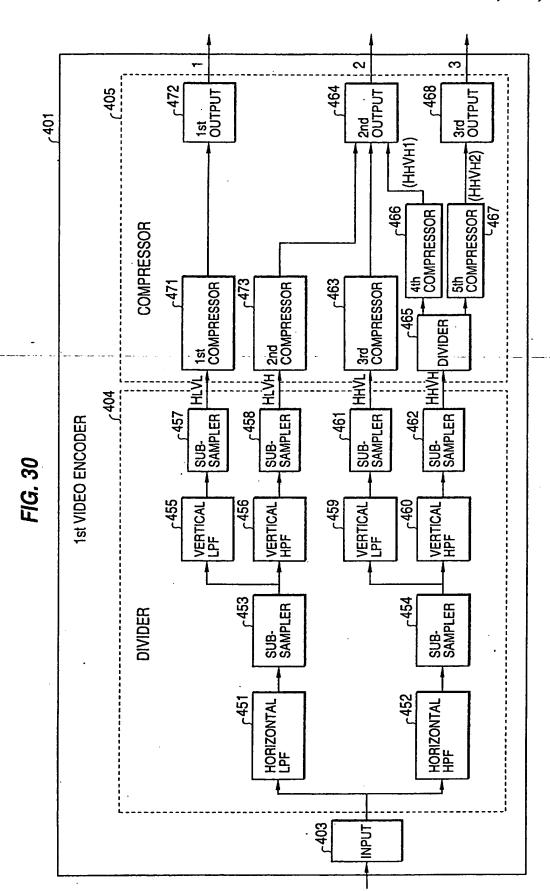
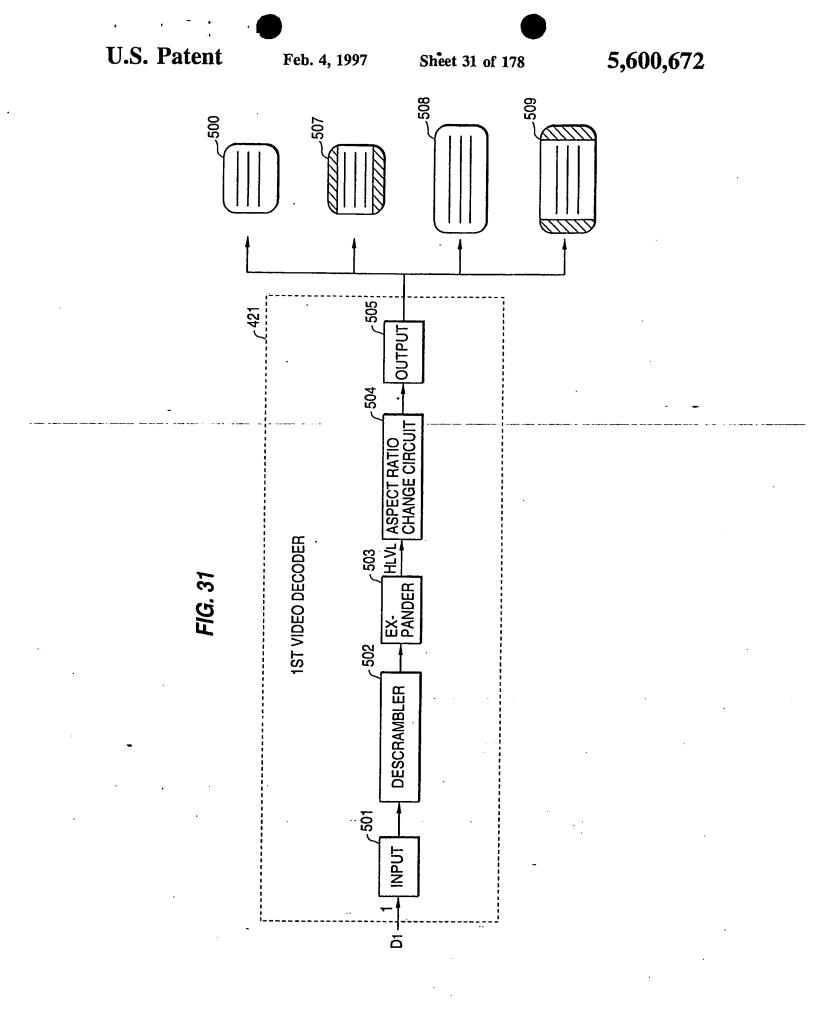


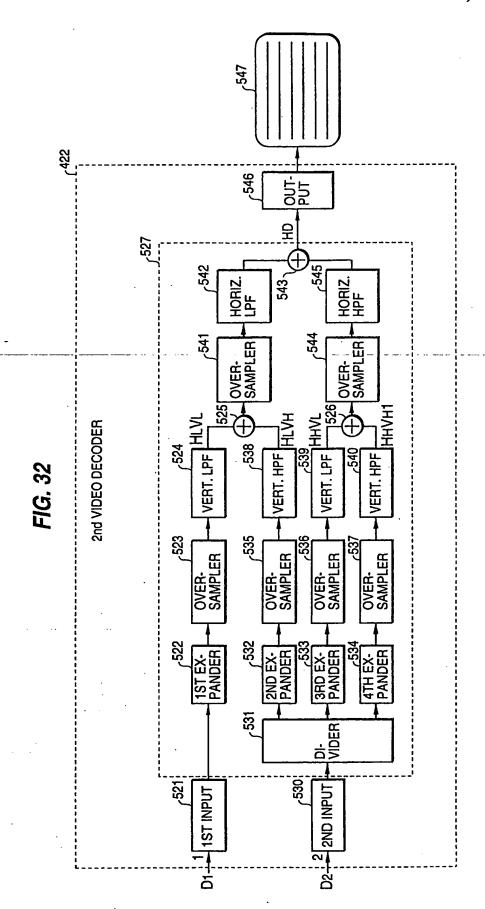
FIG. 28

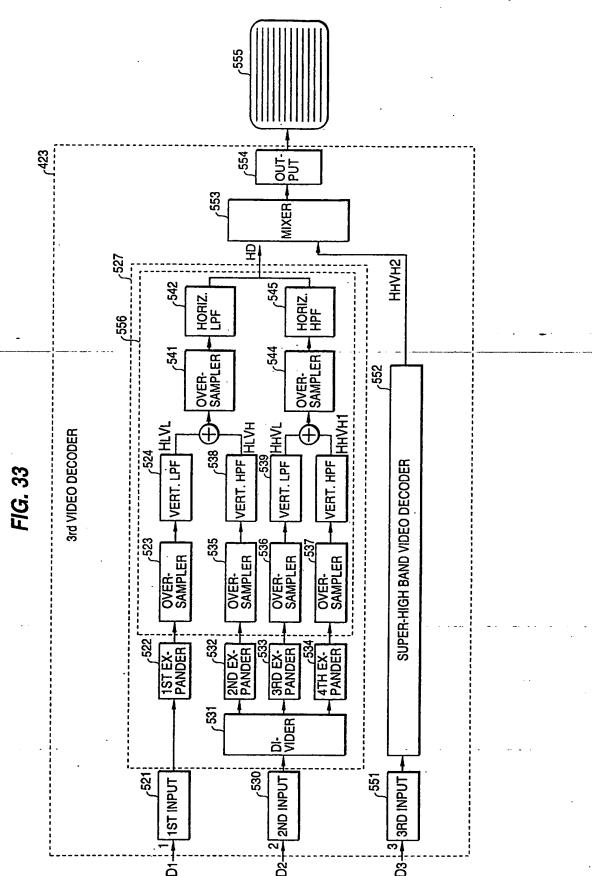


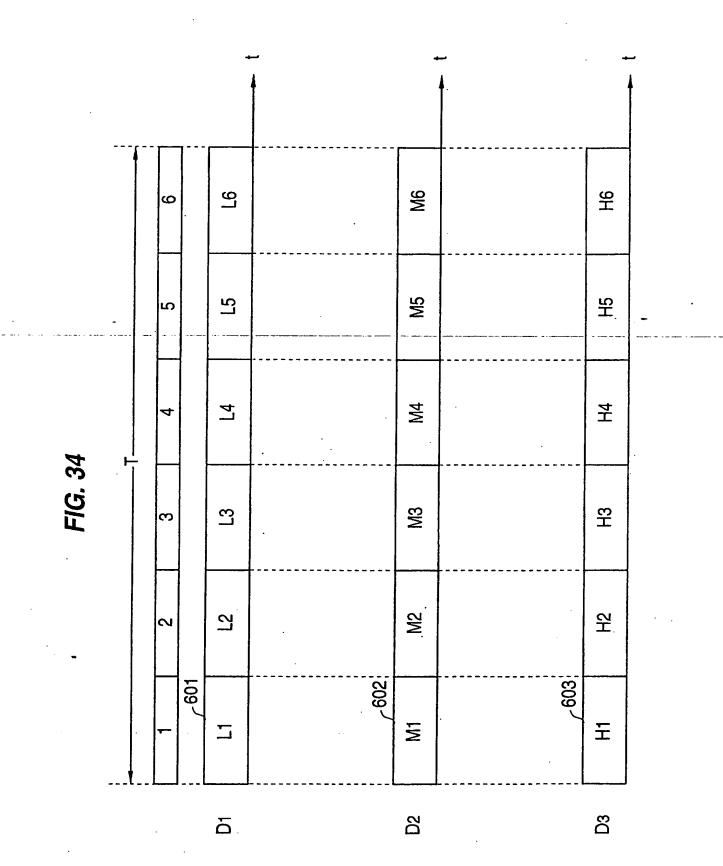


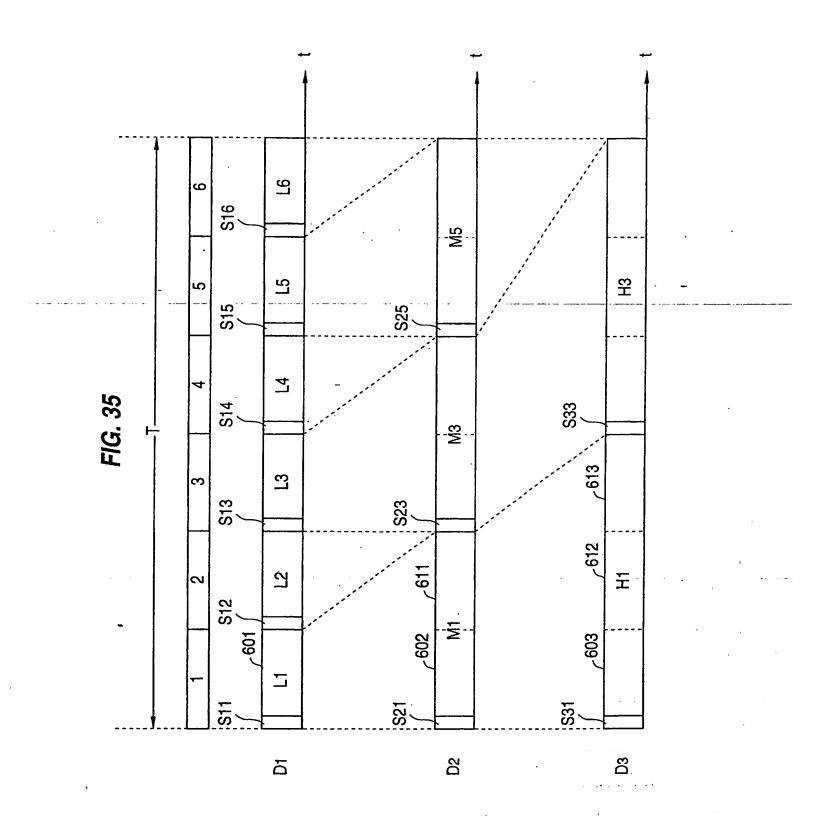


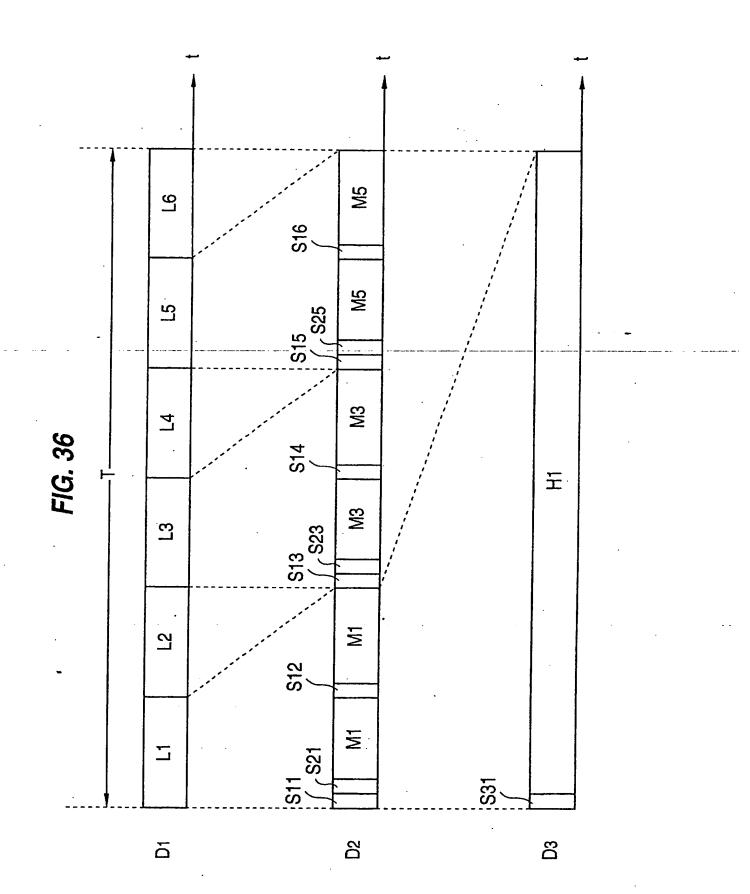












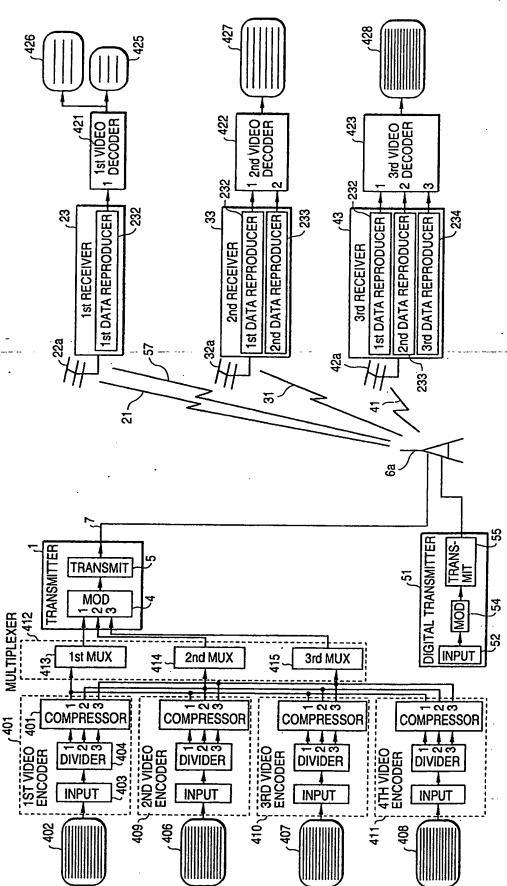
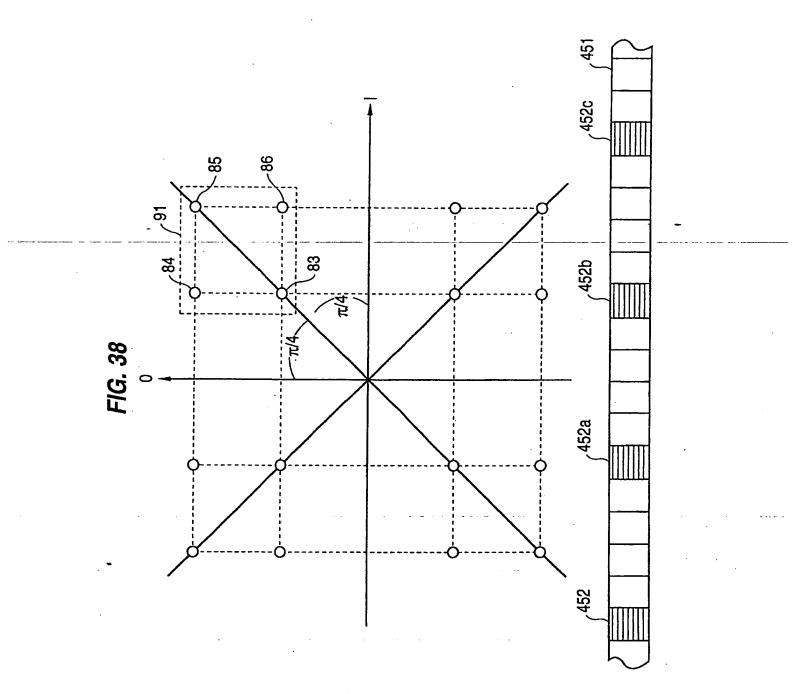
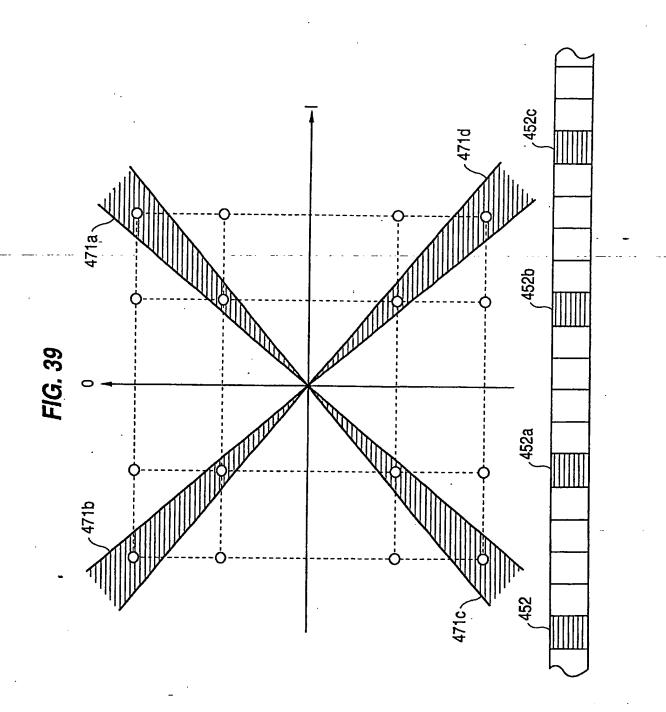


FIG. 37





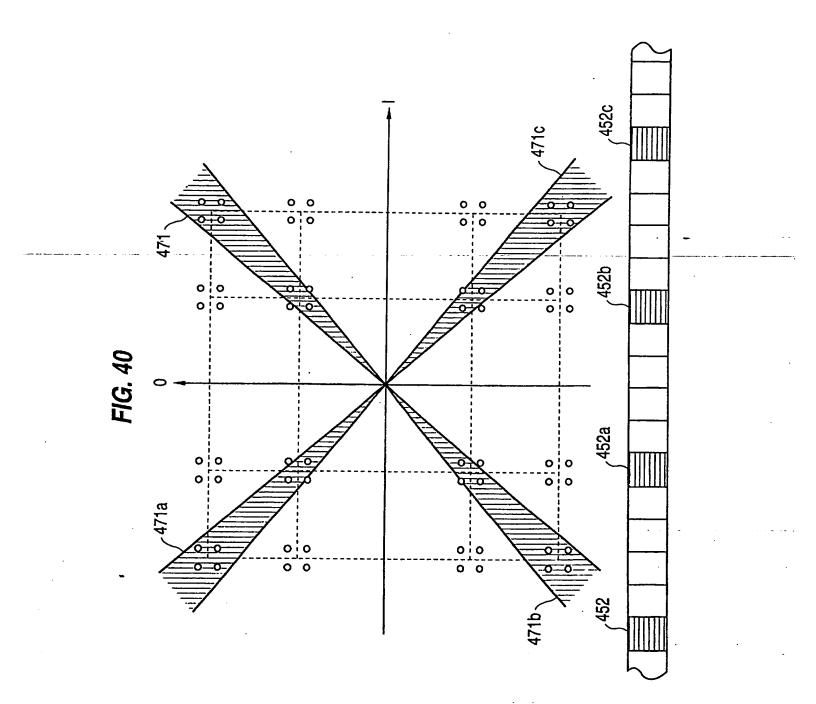


FIG. 41

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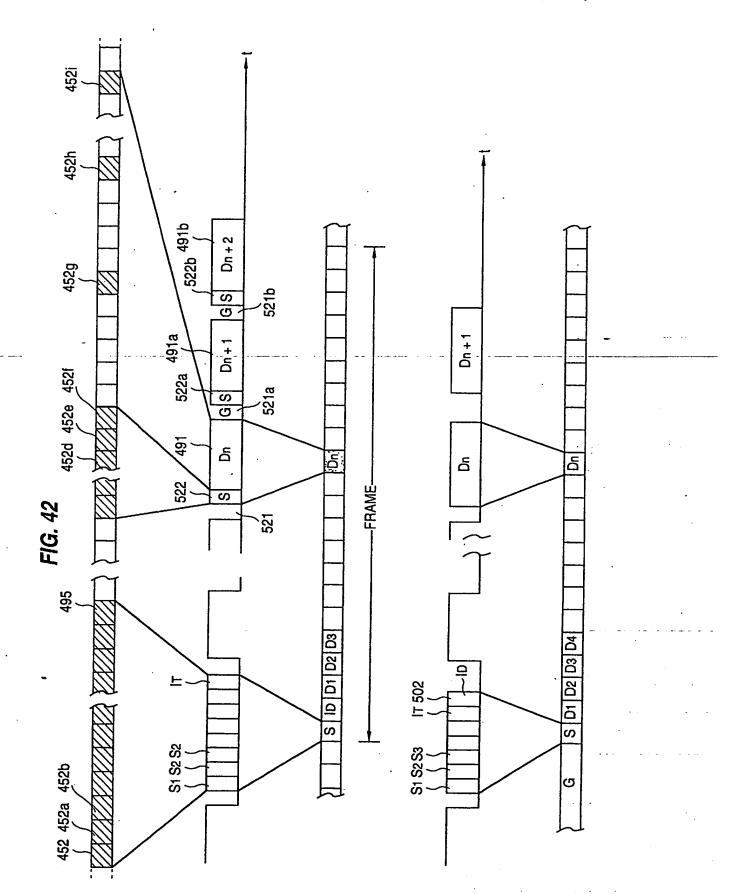
-FRAME-

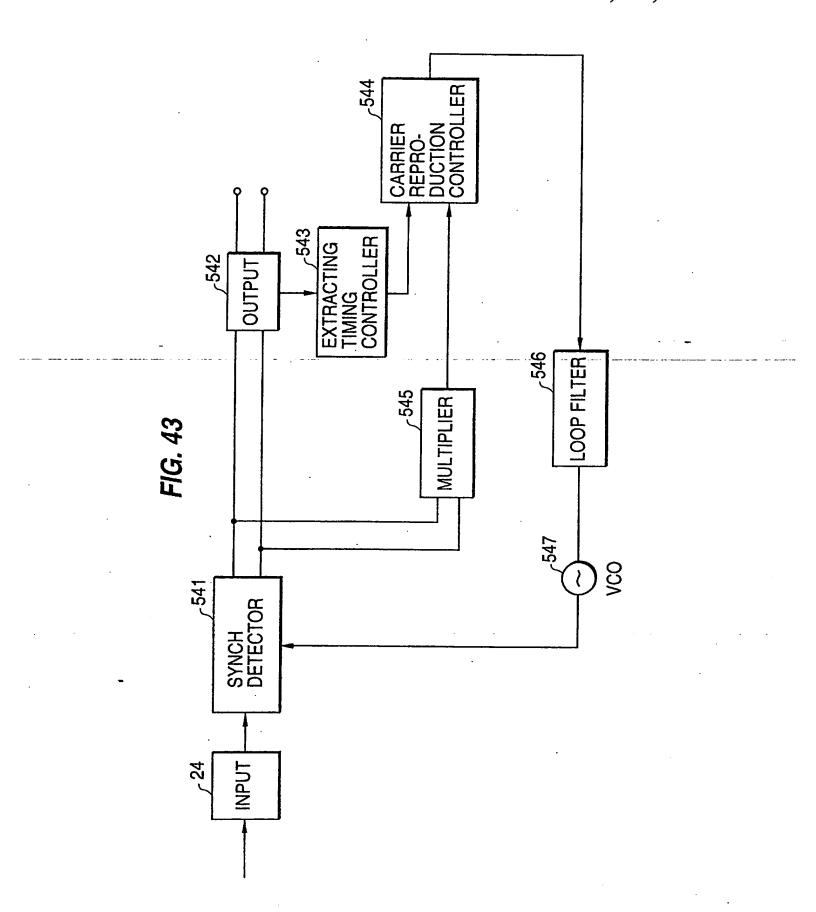
502

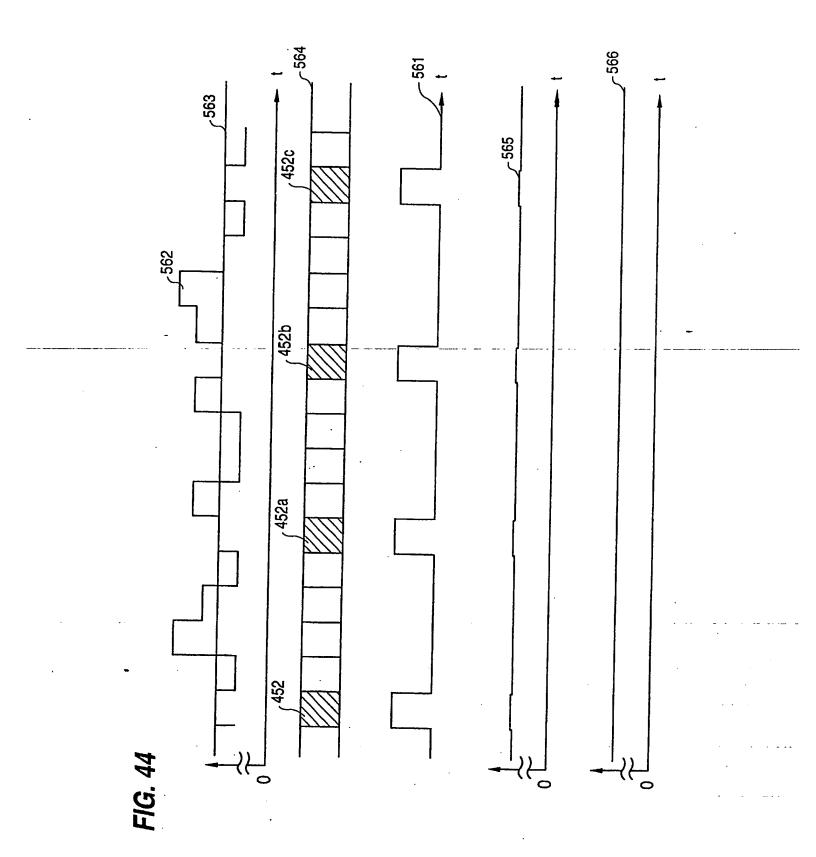
(S2(S0 IT)

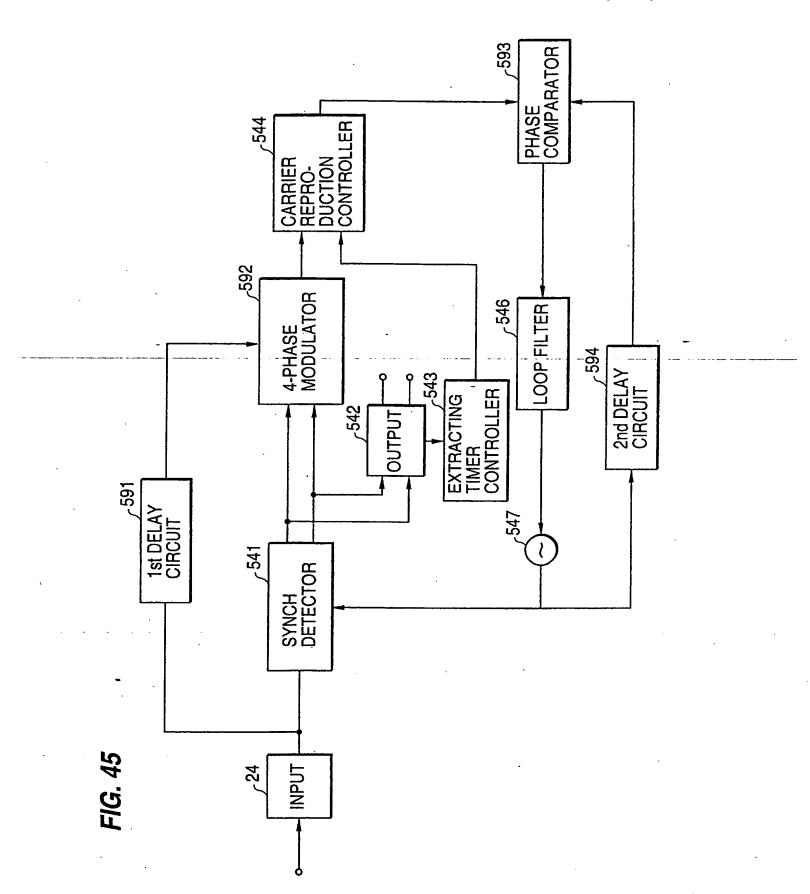
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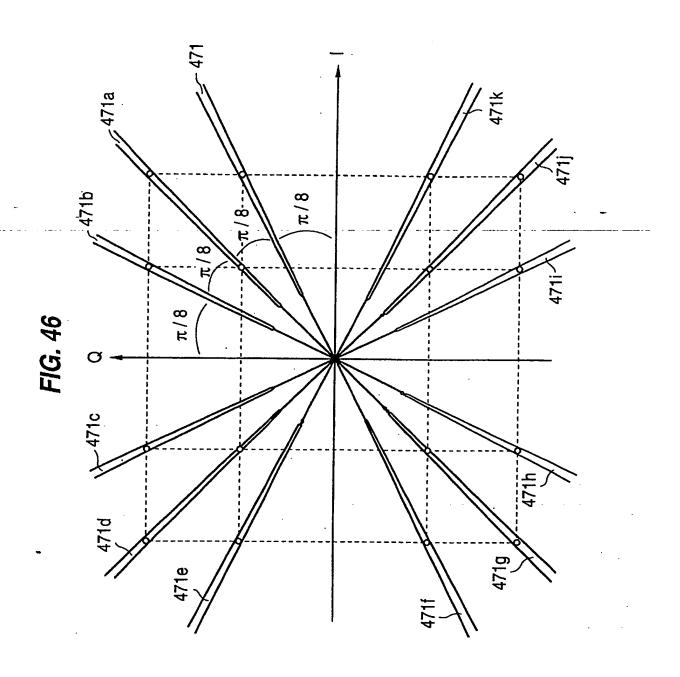








feb. 4, 1997



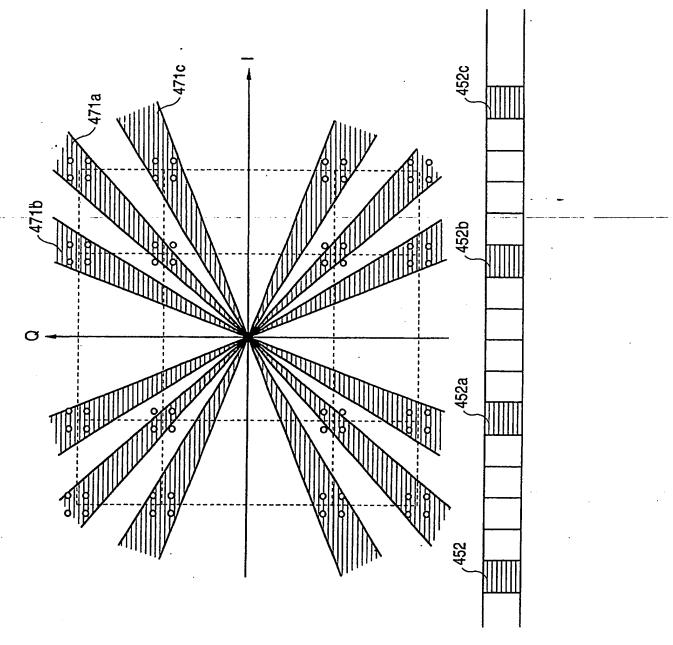


FIG. 47

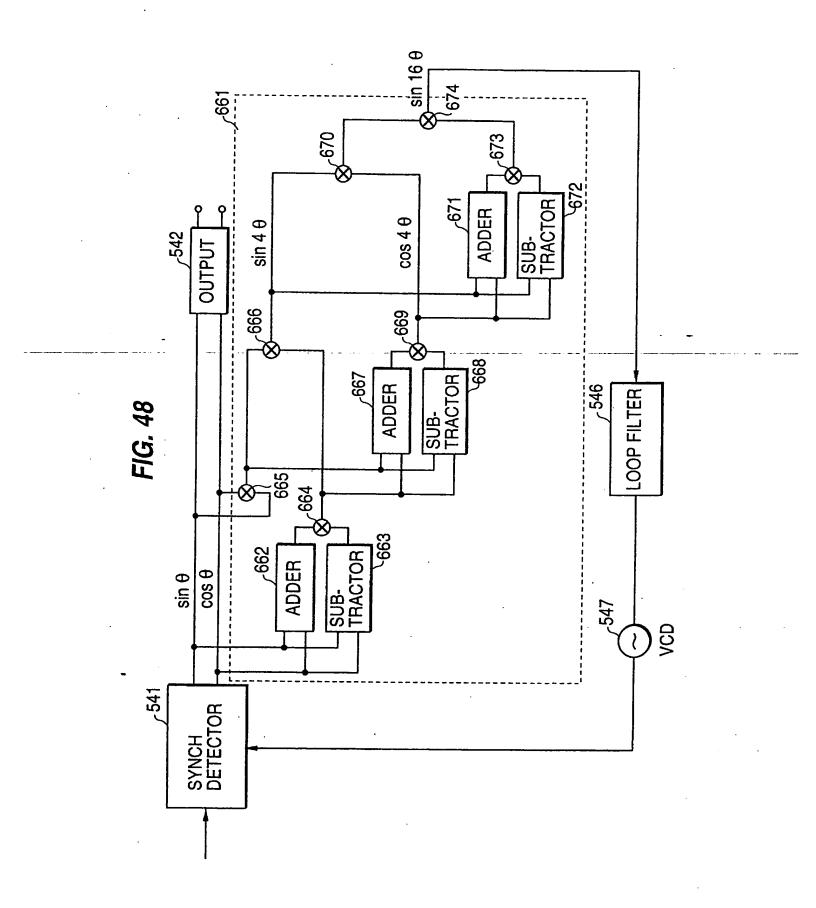
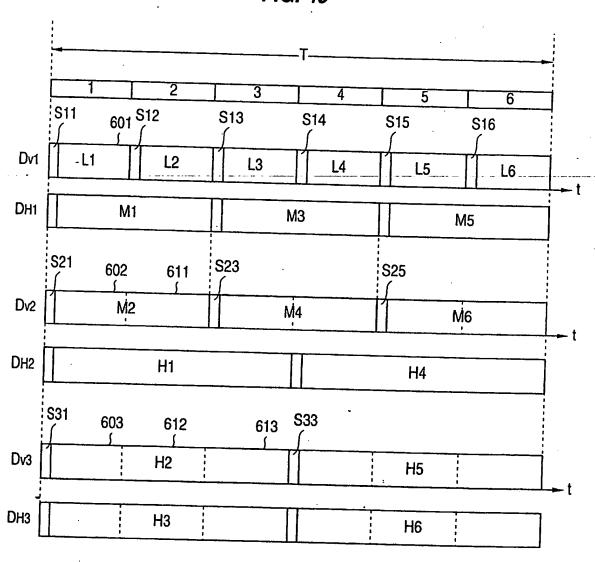
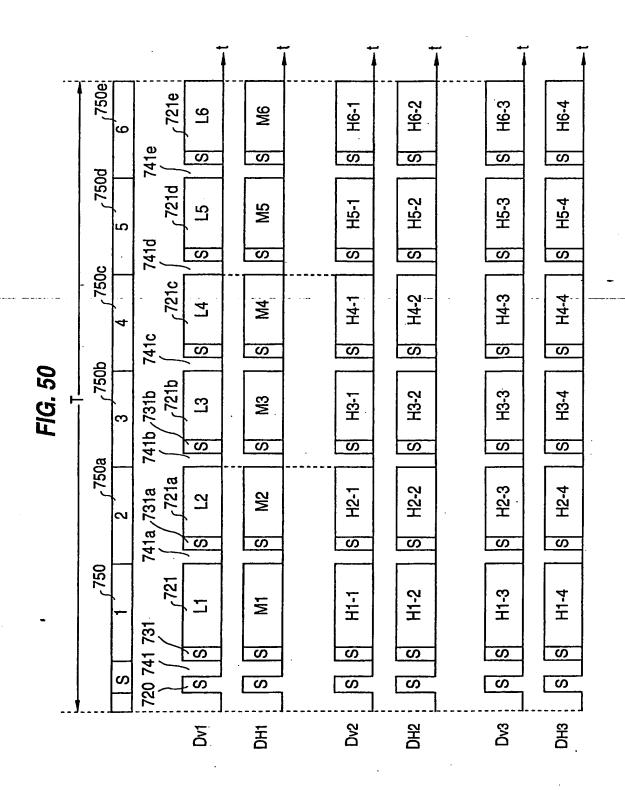
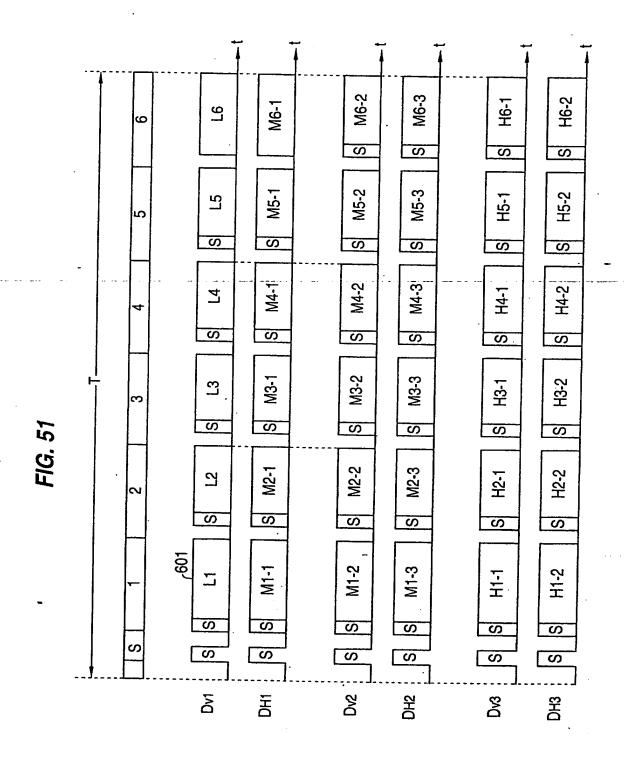
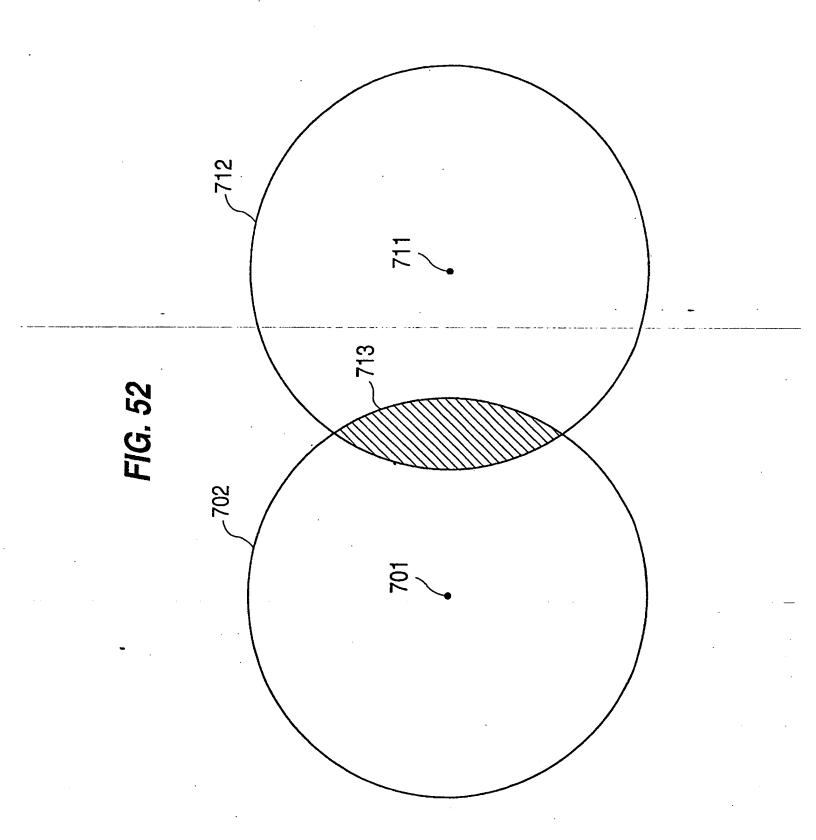


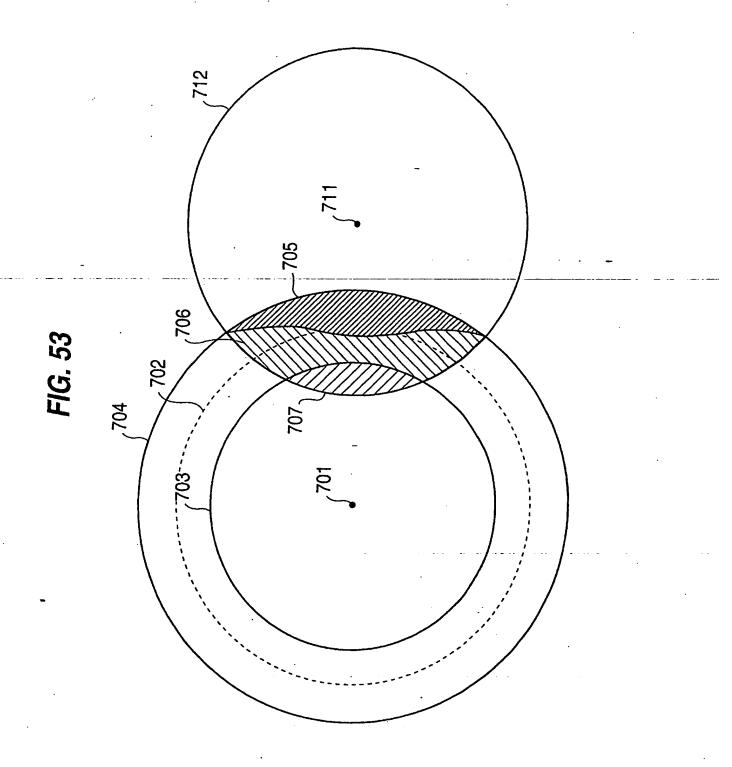
FIG. 49

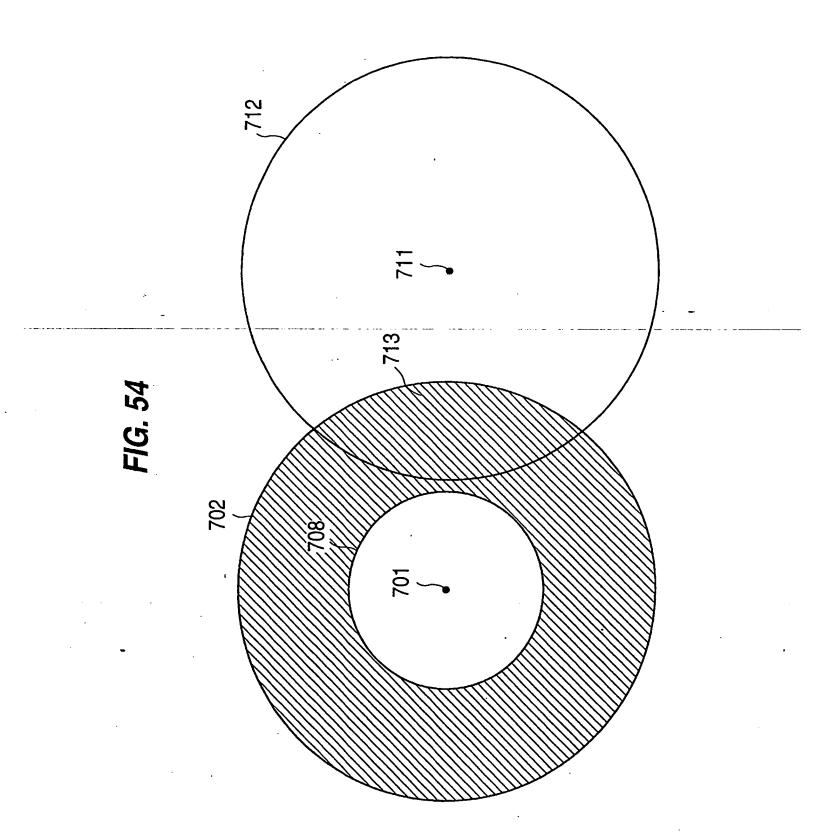


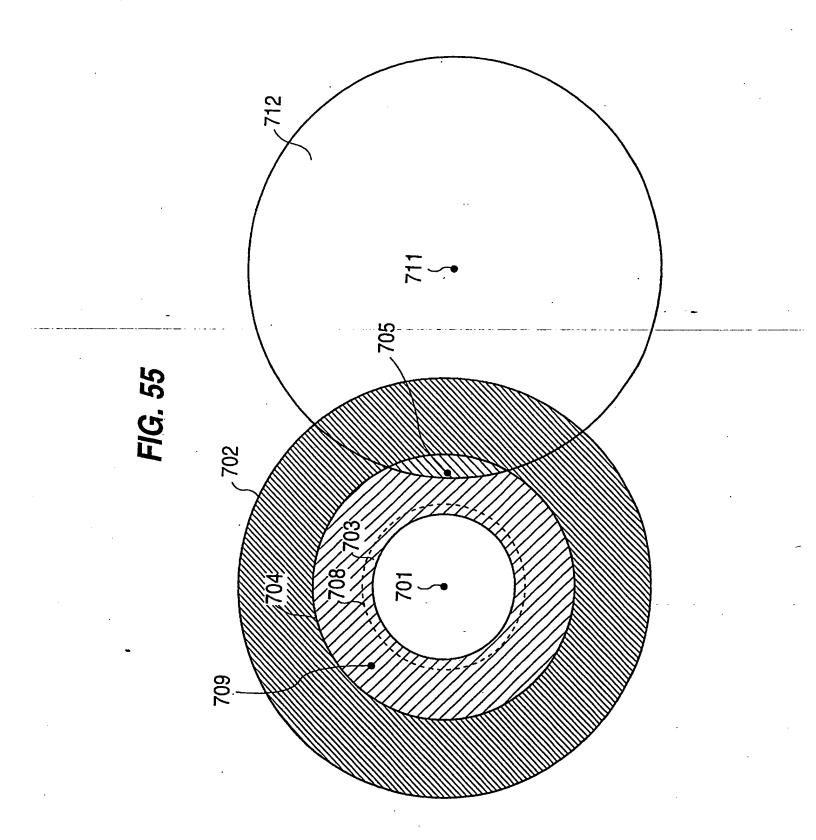












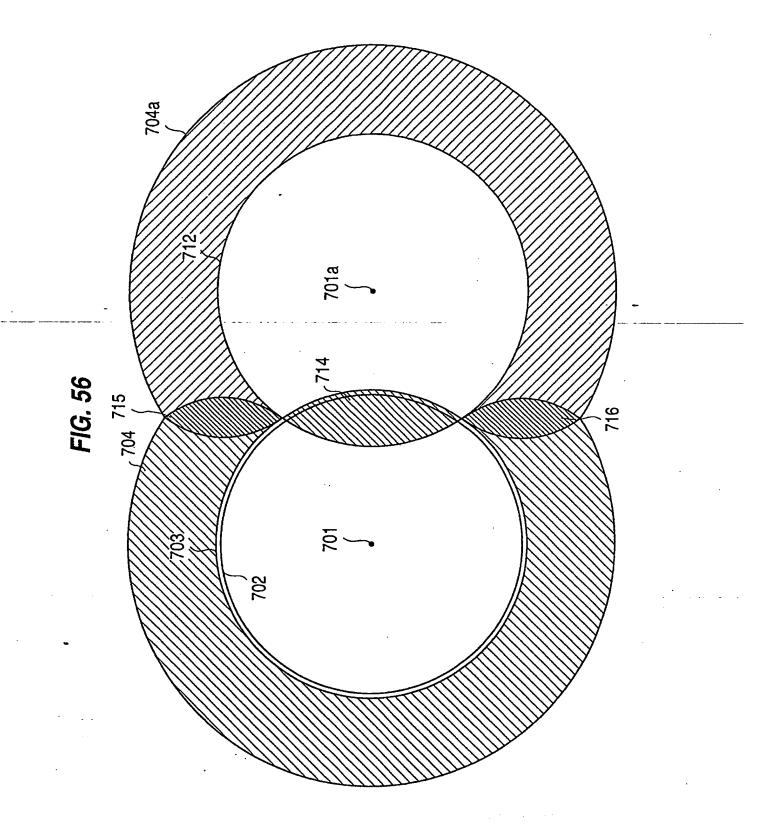


FIG. 57

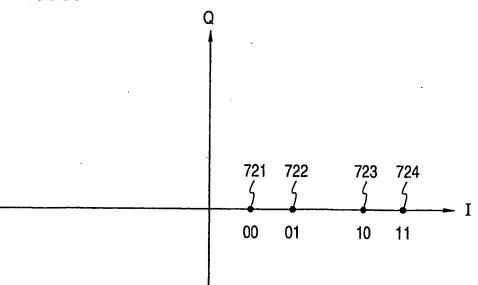
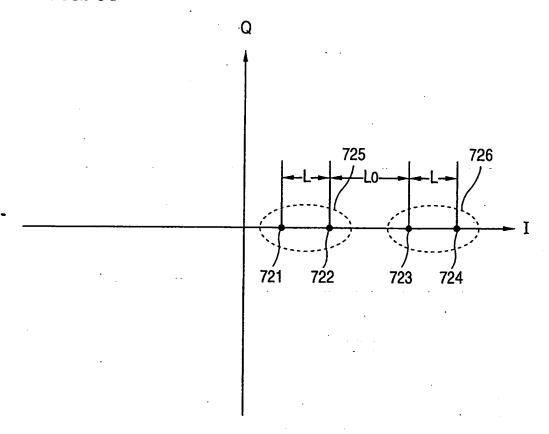
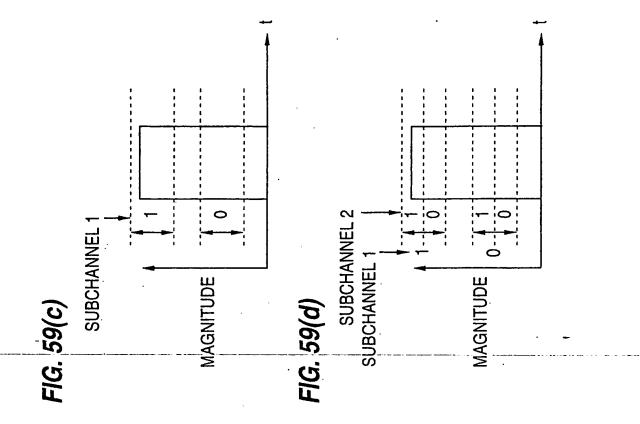
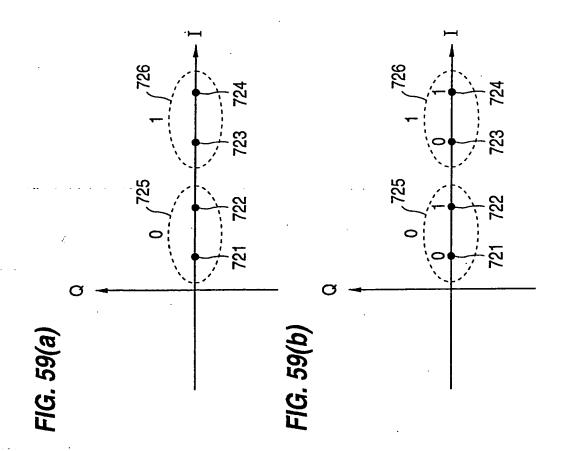
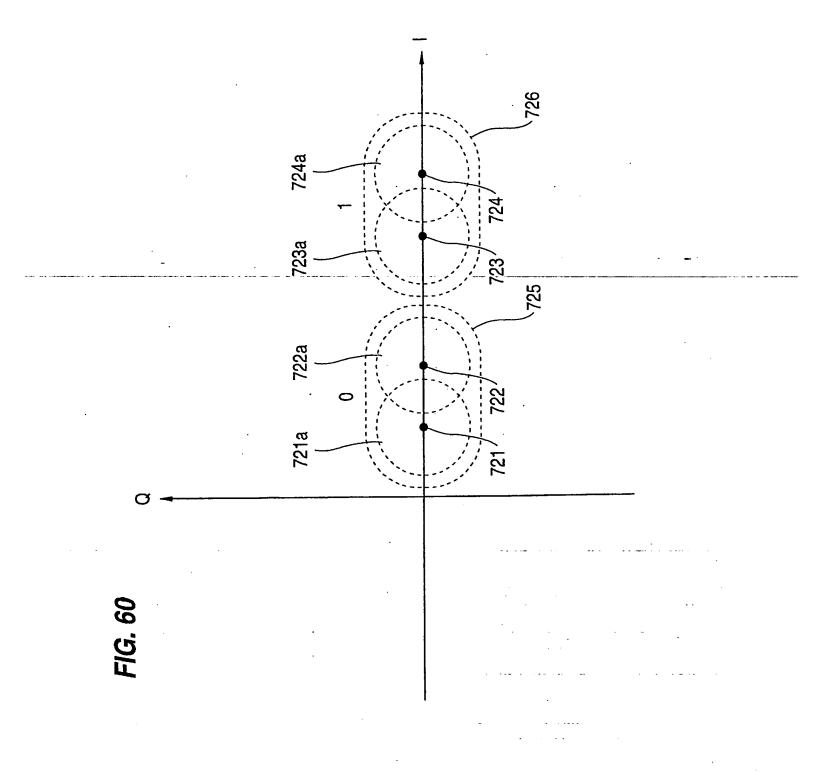


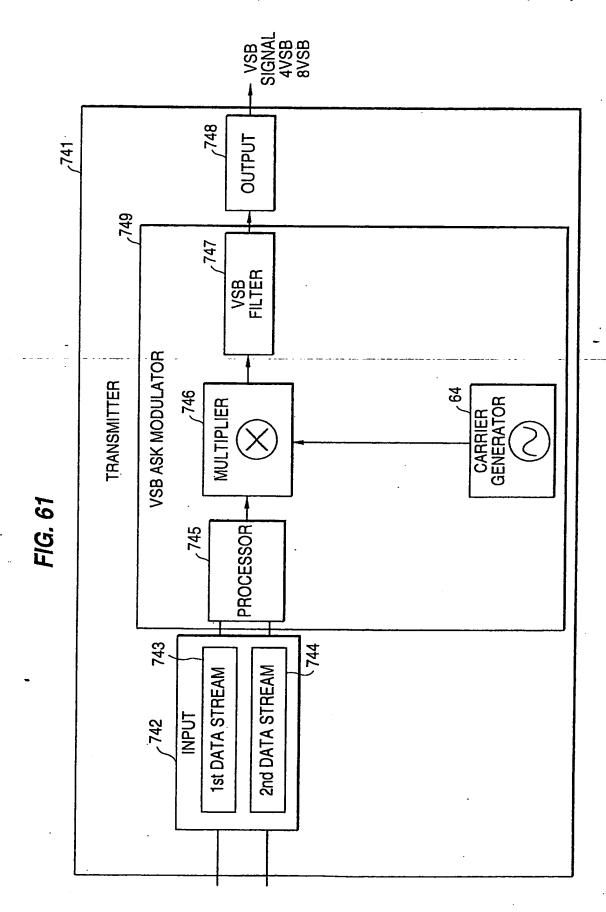
FIG. 58

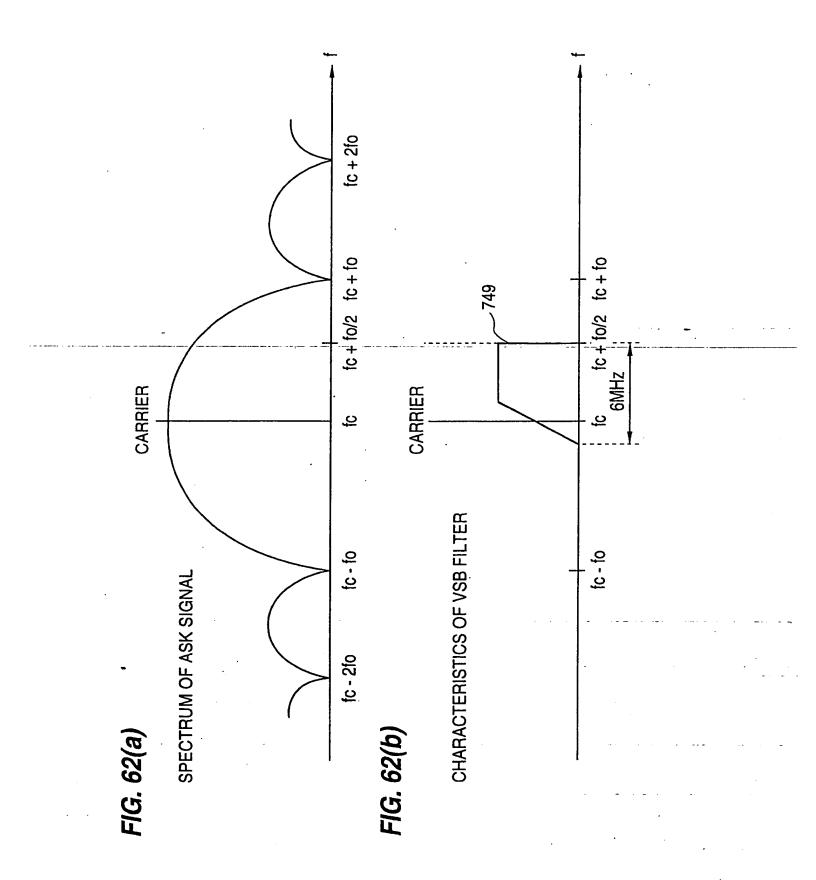


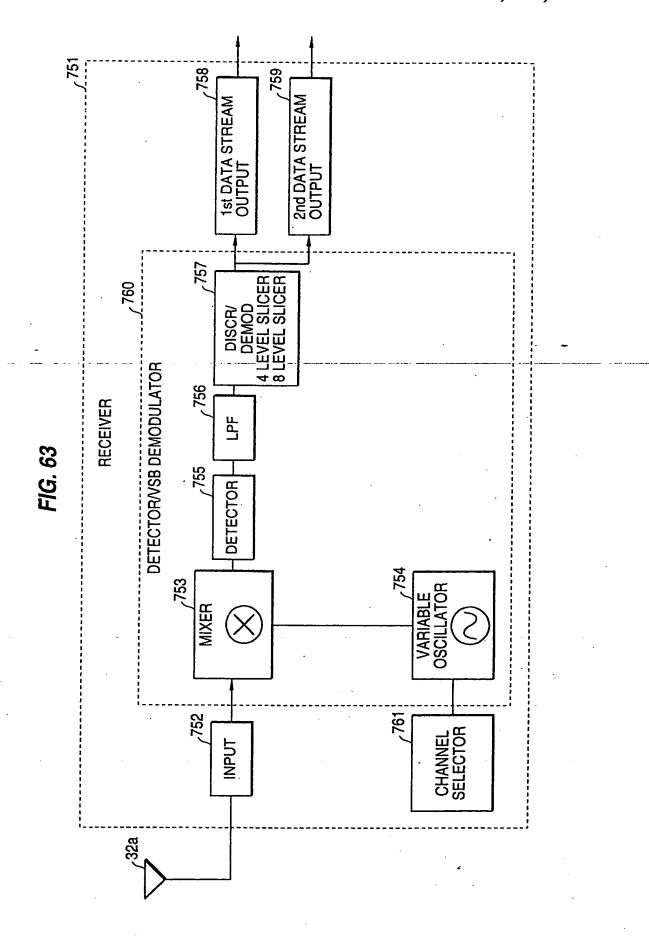


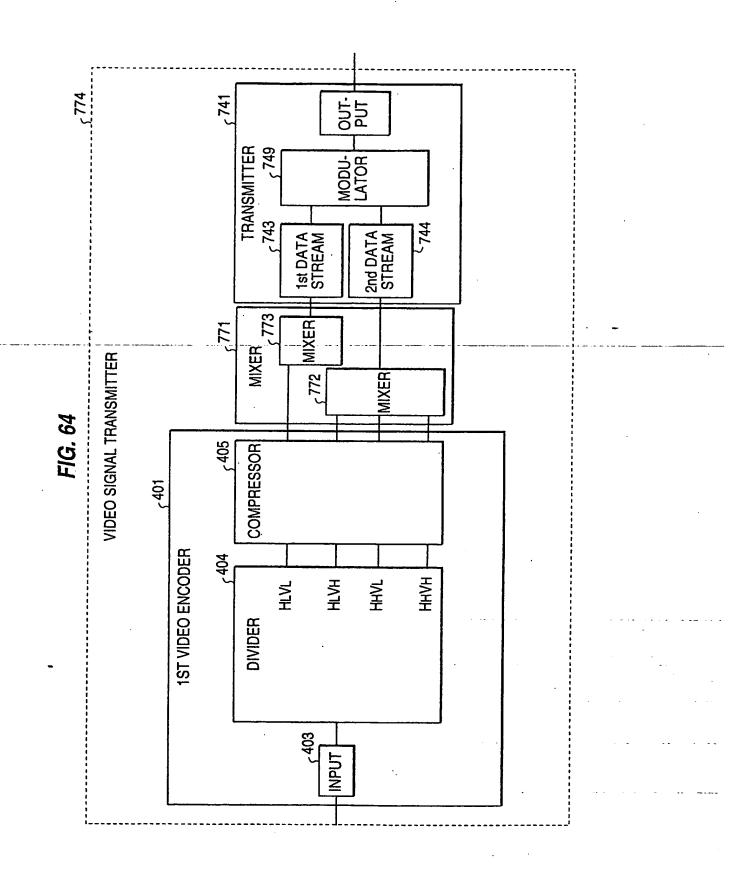


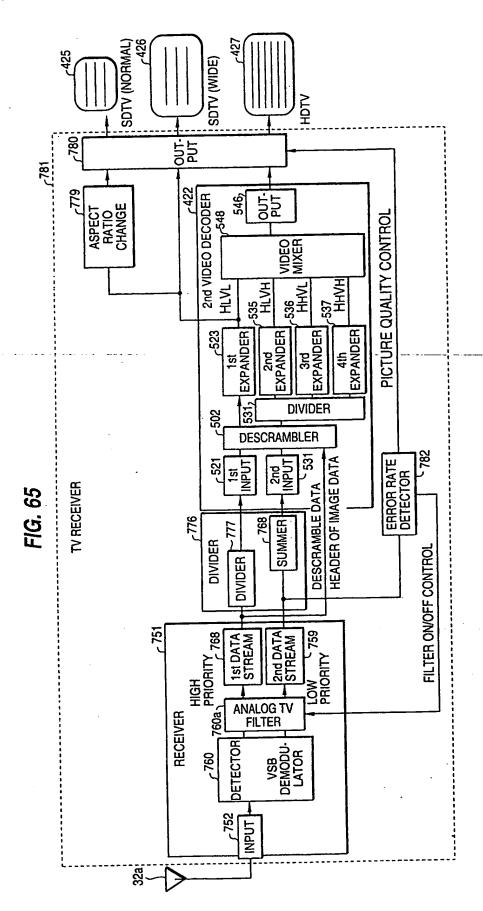


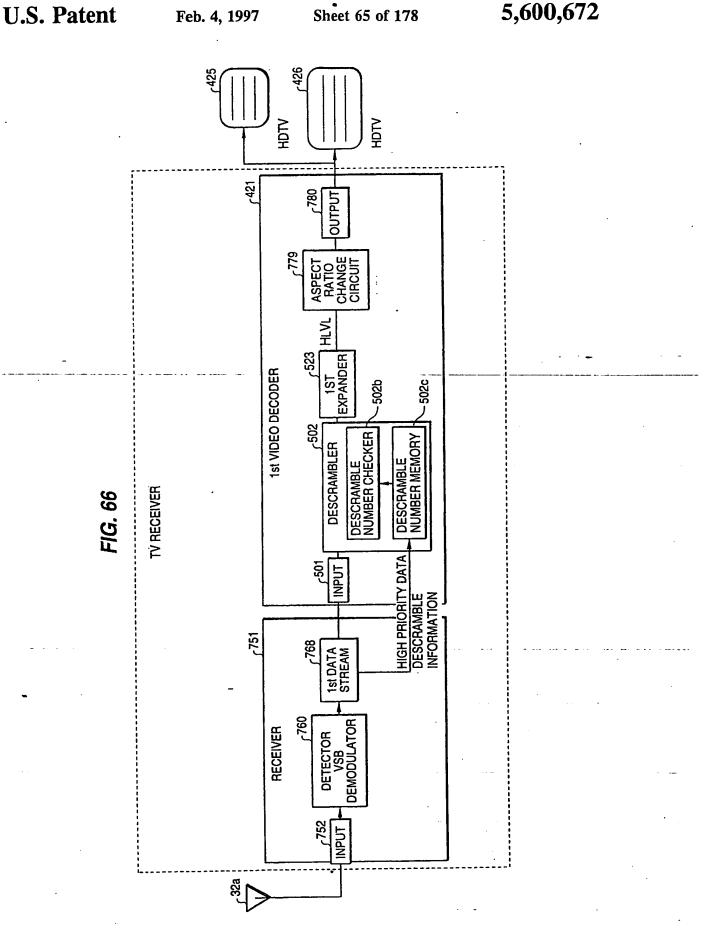


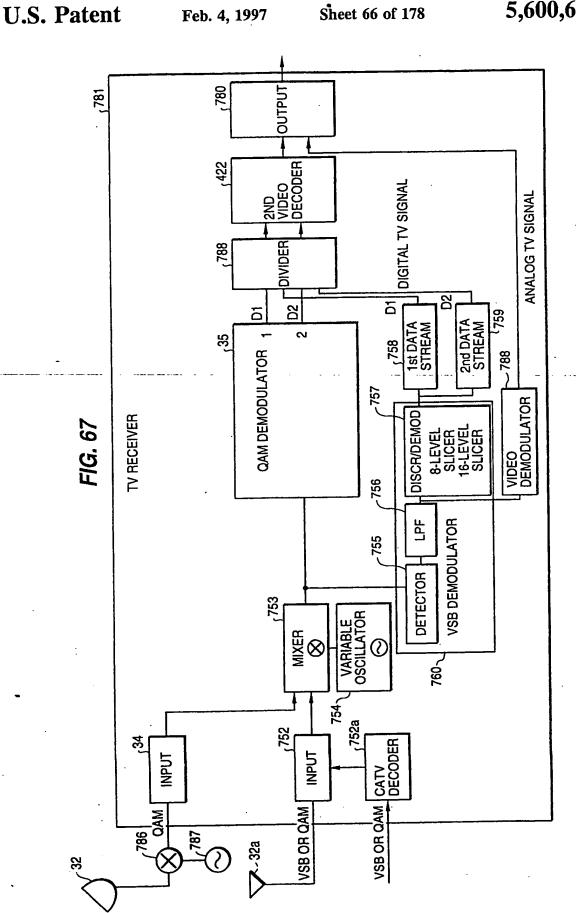


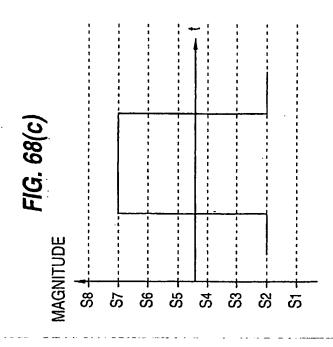


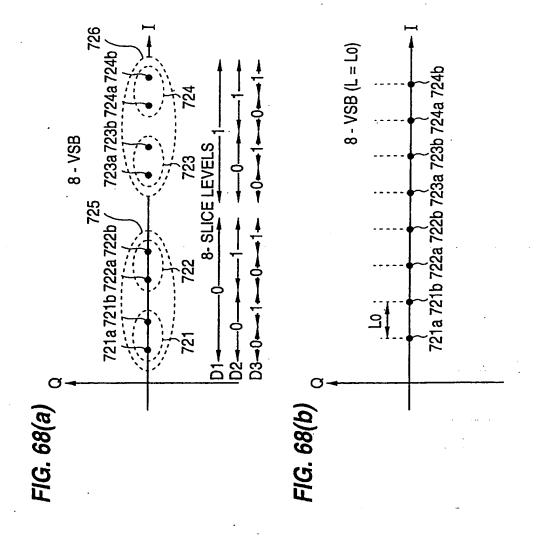


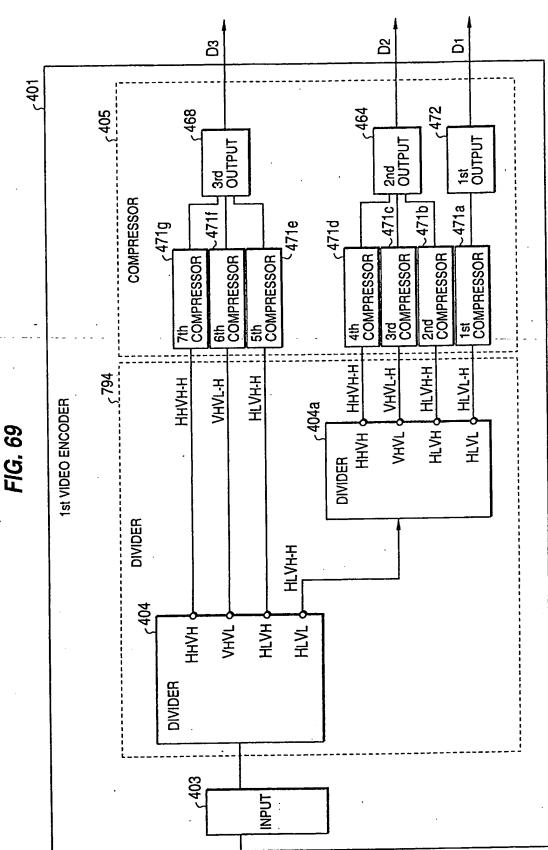


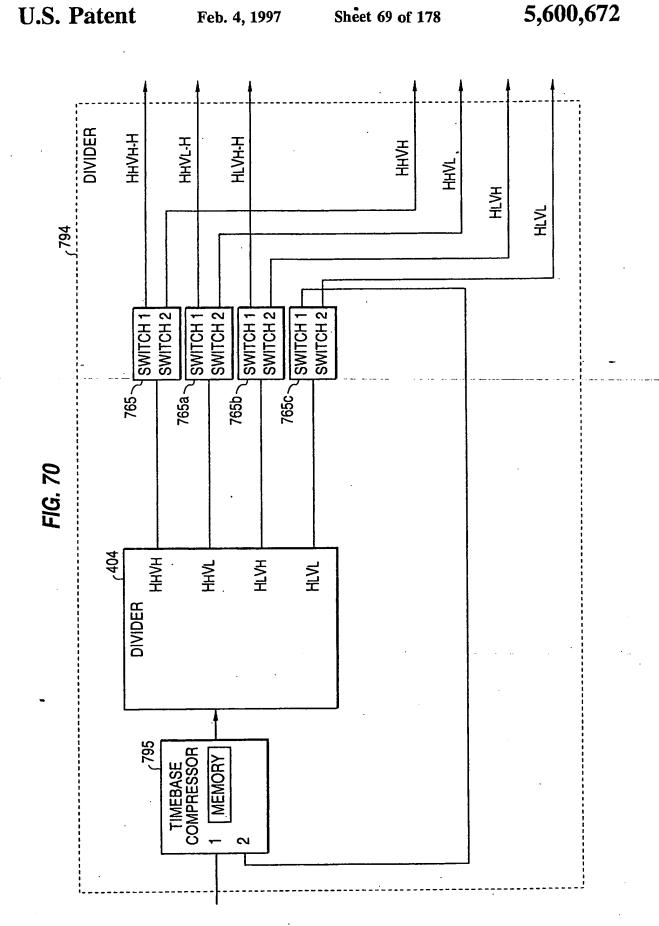


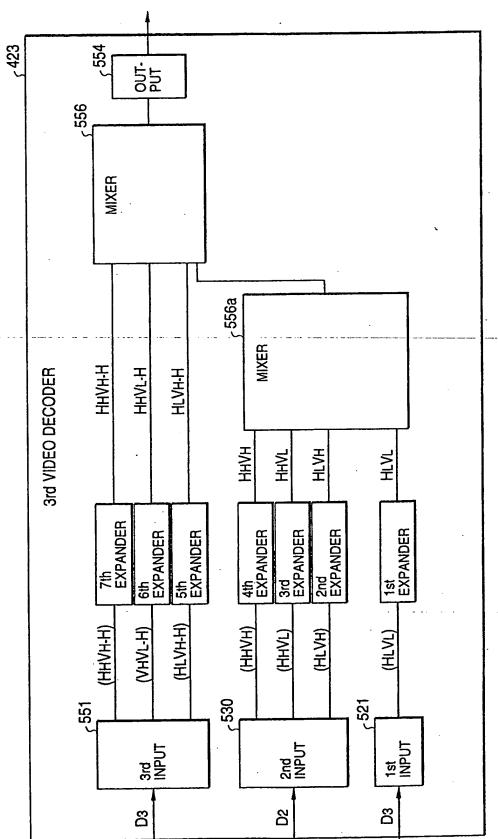












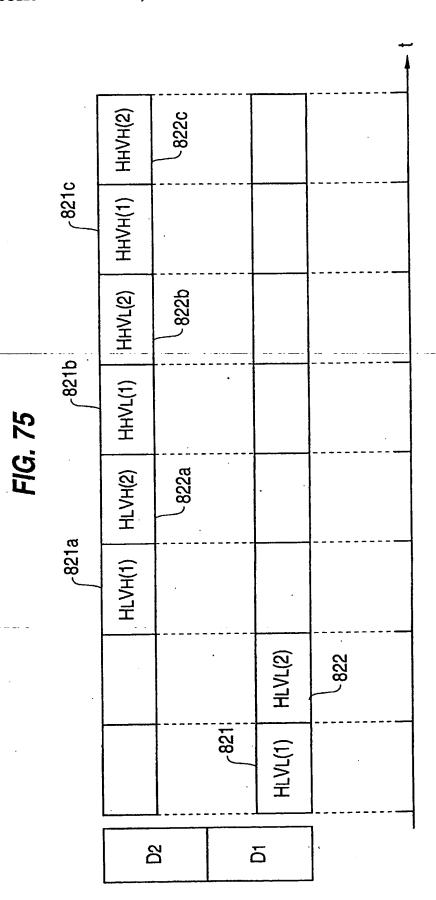
554 PUT. H_VH ¥ F H./L 765a 765b .765c 1, SWITCH зwiтсн SWITCH switch 3rd VIDEO DECODER -522d HLVH-H 522c HHVH 522b HHVL .522 H.VL 7th EXPANDER 6th EXPANDER 3rd EXPANDER 2nd EXPANDER 1st EXPANDER 5th EXPANDER 4th EXPANDER (HLVH-H) (H-H/HH) (ННИН) (HLVH) (HHVL) (HLVL) -530 521 551 2nd INPUT 22 ස ස

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<u></u> ×811c 422 810c 4 HHH **VIDEO MIXER** 9 .810b 2nd VIDEO DECODER क H₹ EXPANDER 7 ,810a -812 SWITCH ಭ 보XH 口 530 2nd INPUT 1st INPUT 二 H/L FIG. 74(b) ₽. 5 D2 5



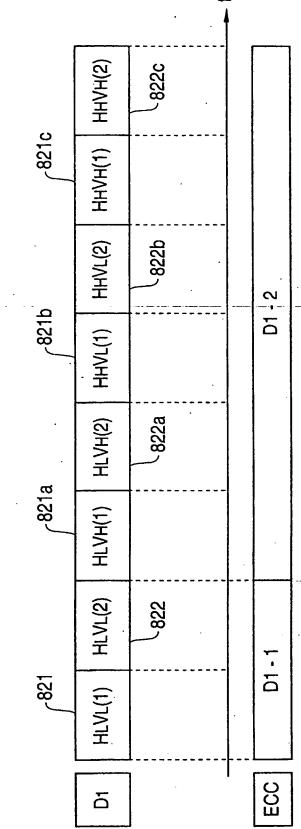
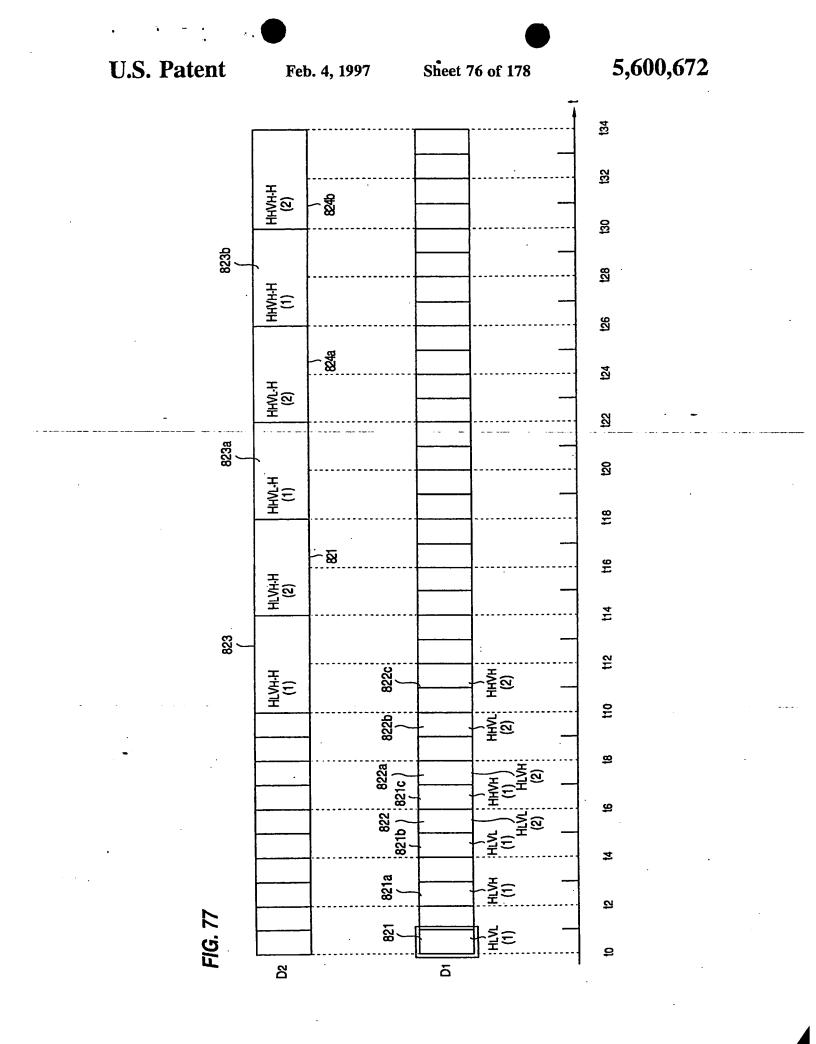
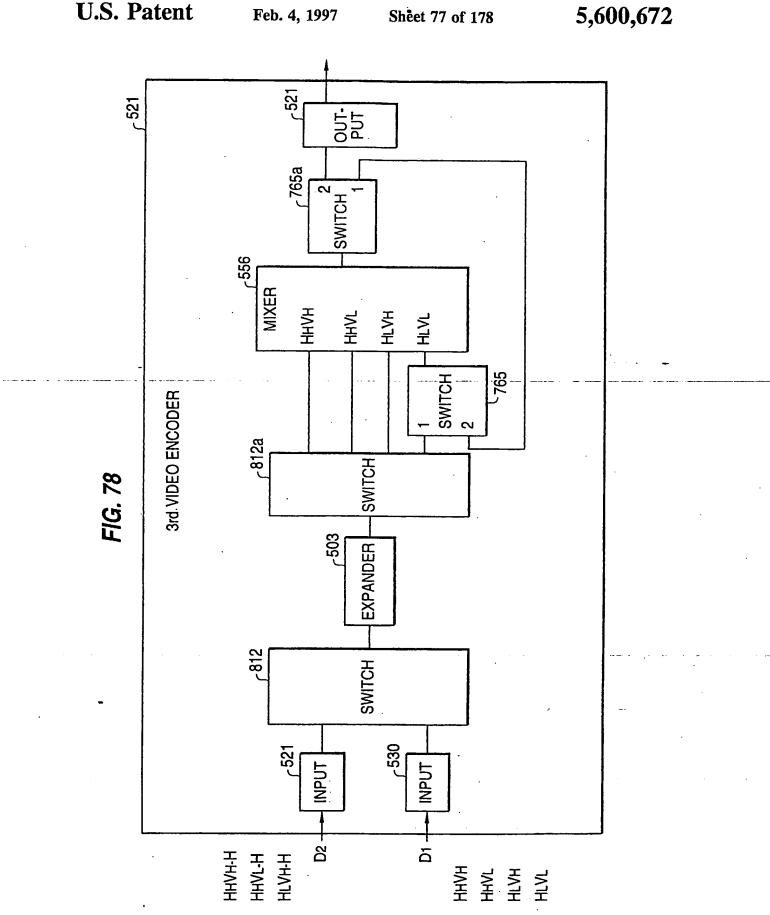
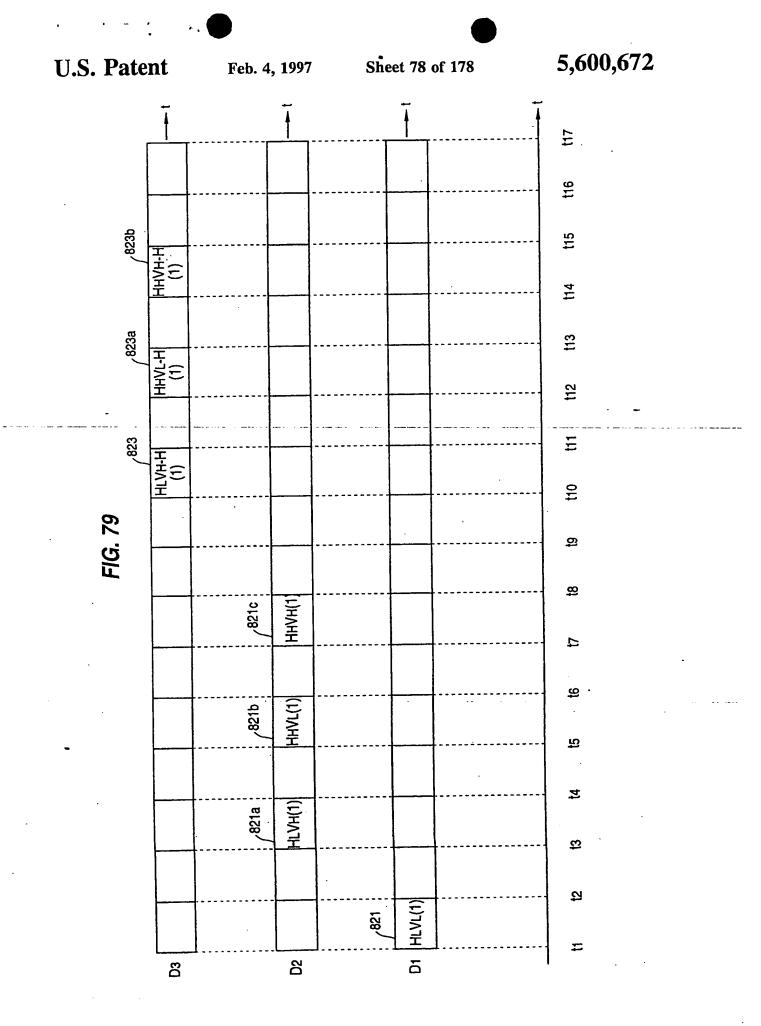
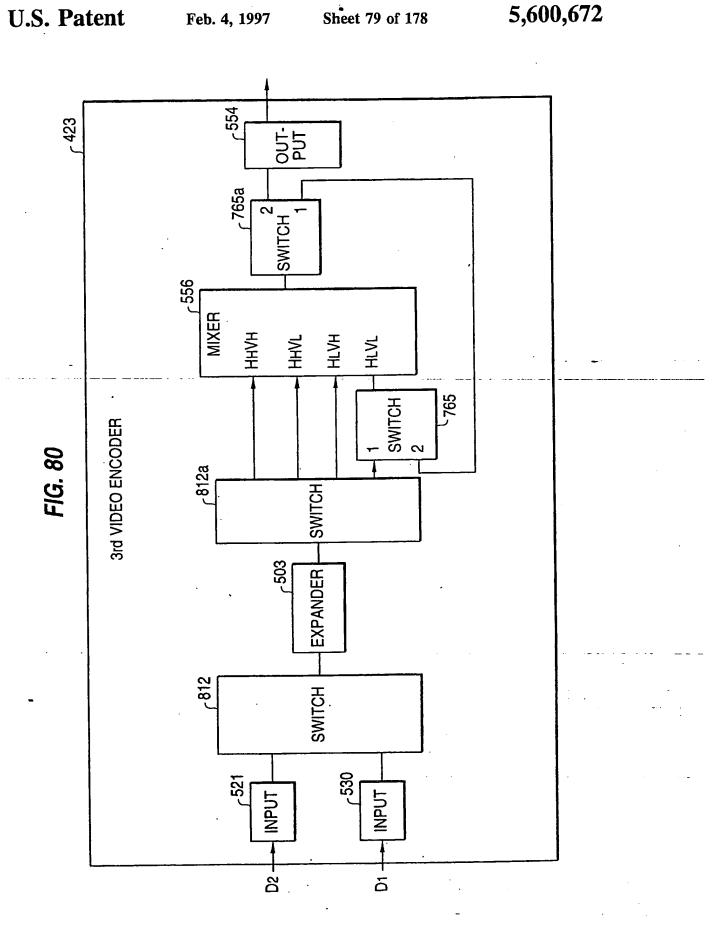


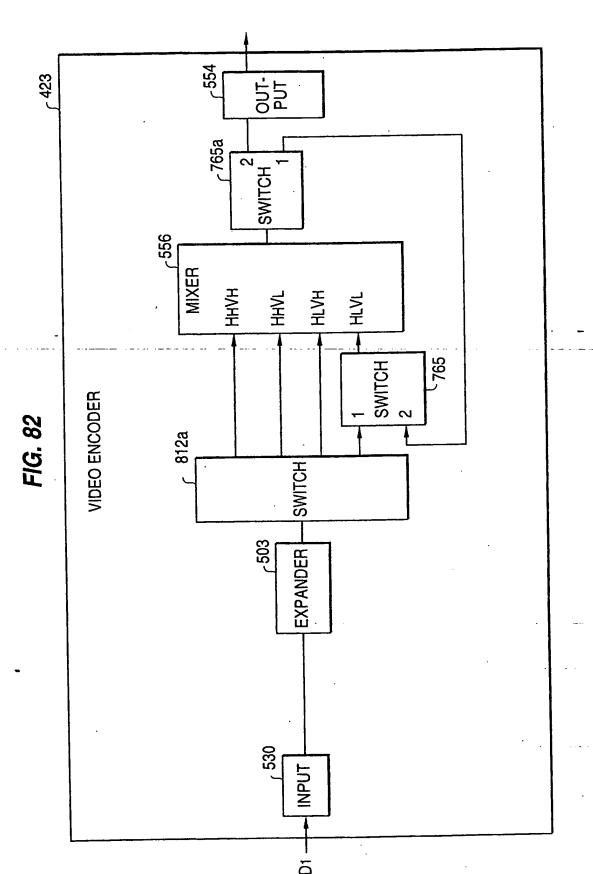
FIG. 76



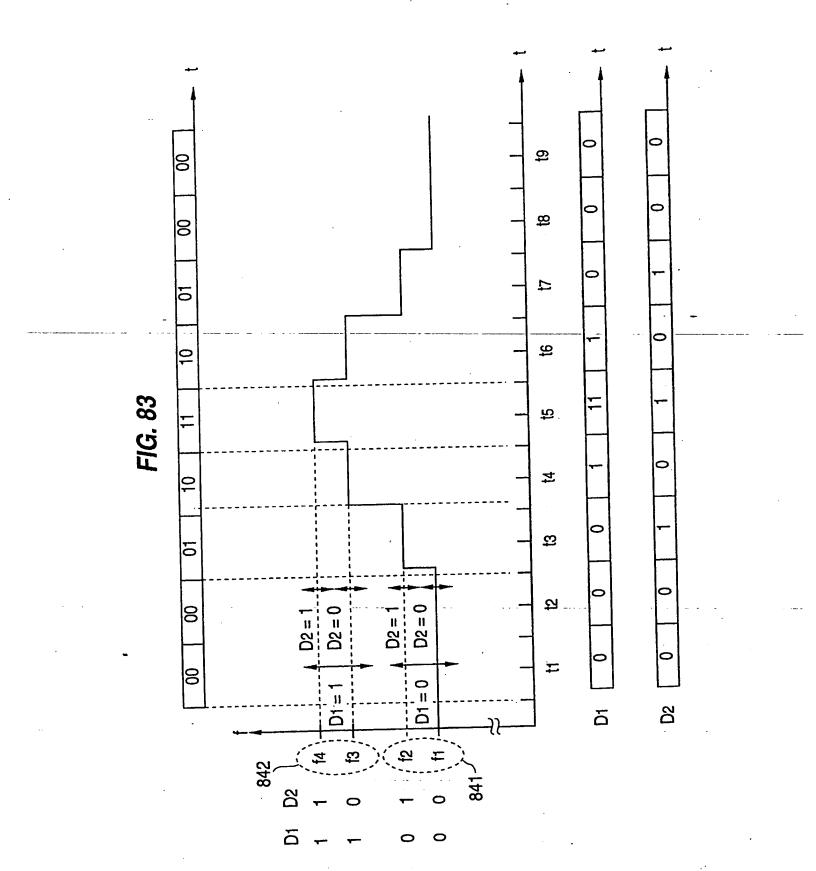


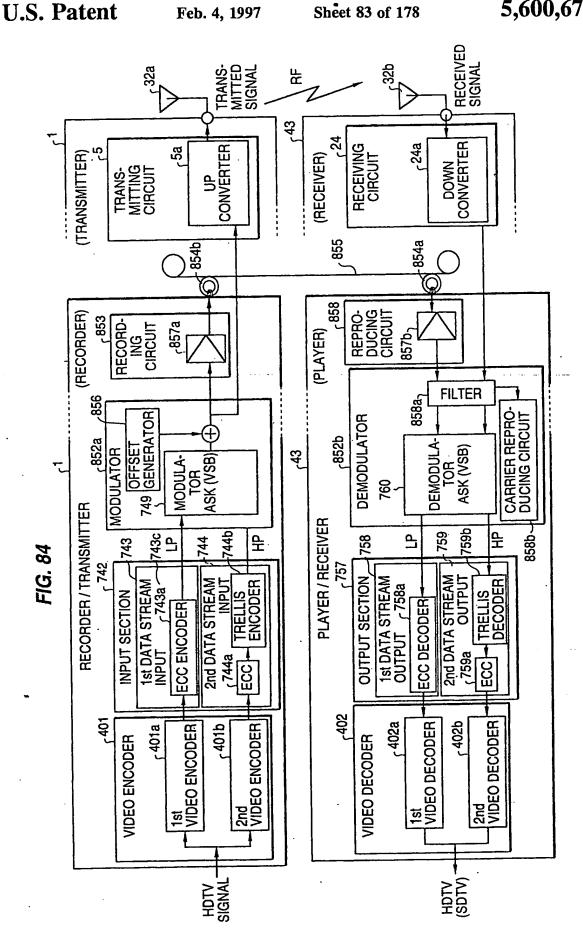


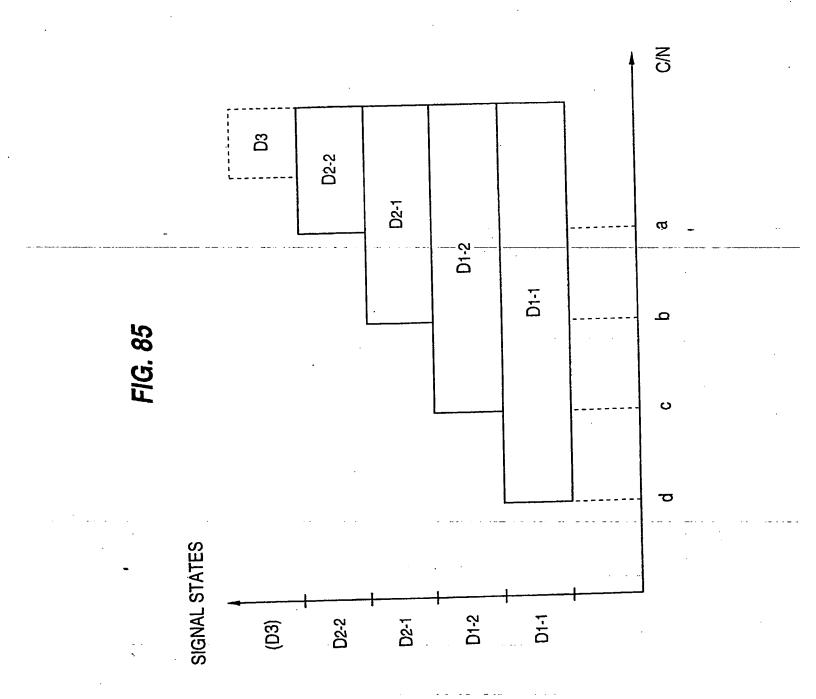


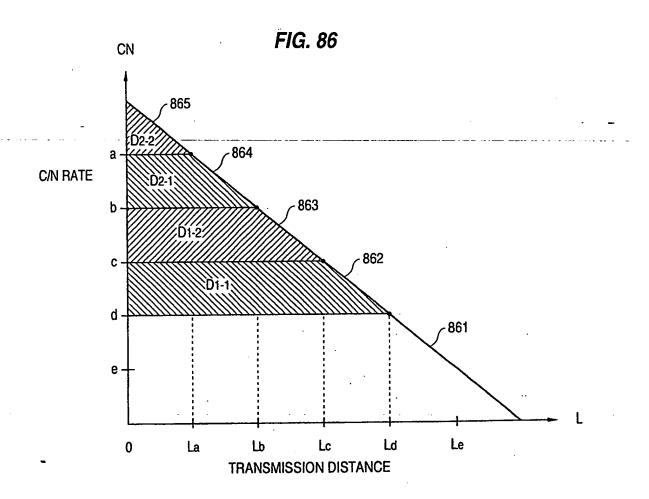


Sheet 82 of 178









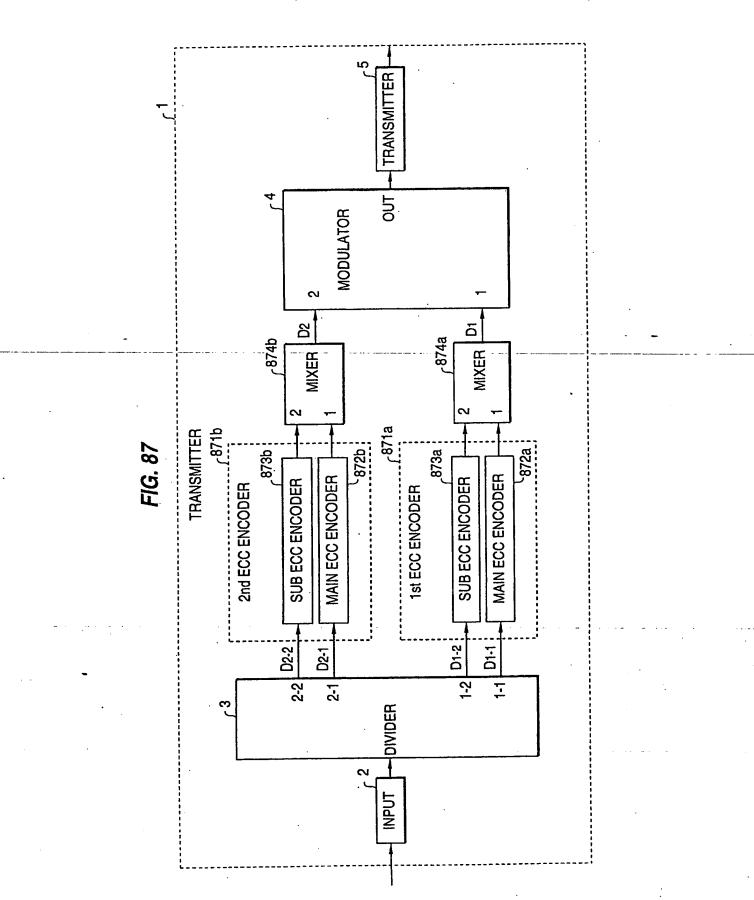
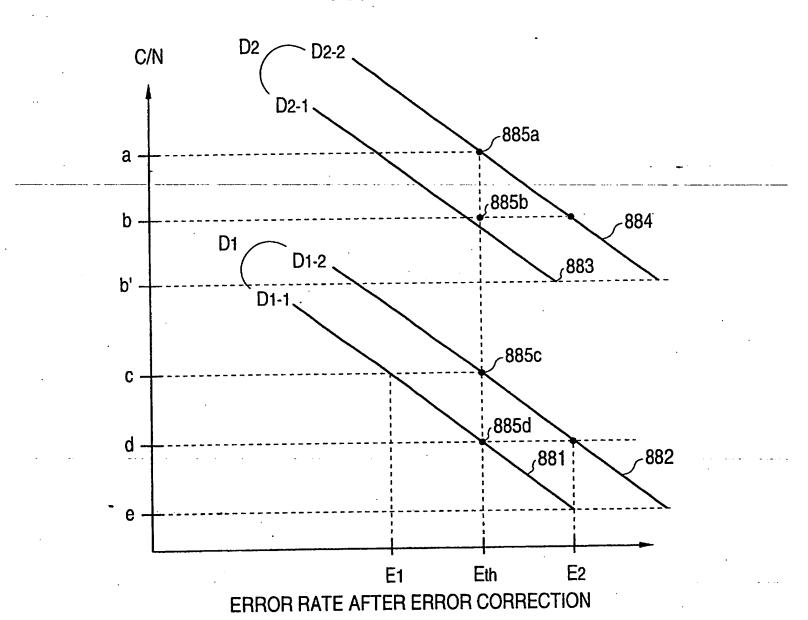
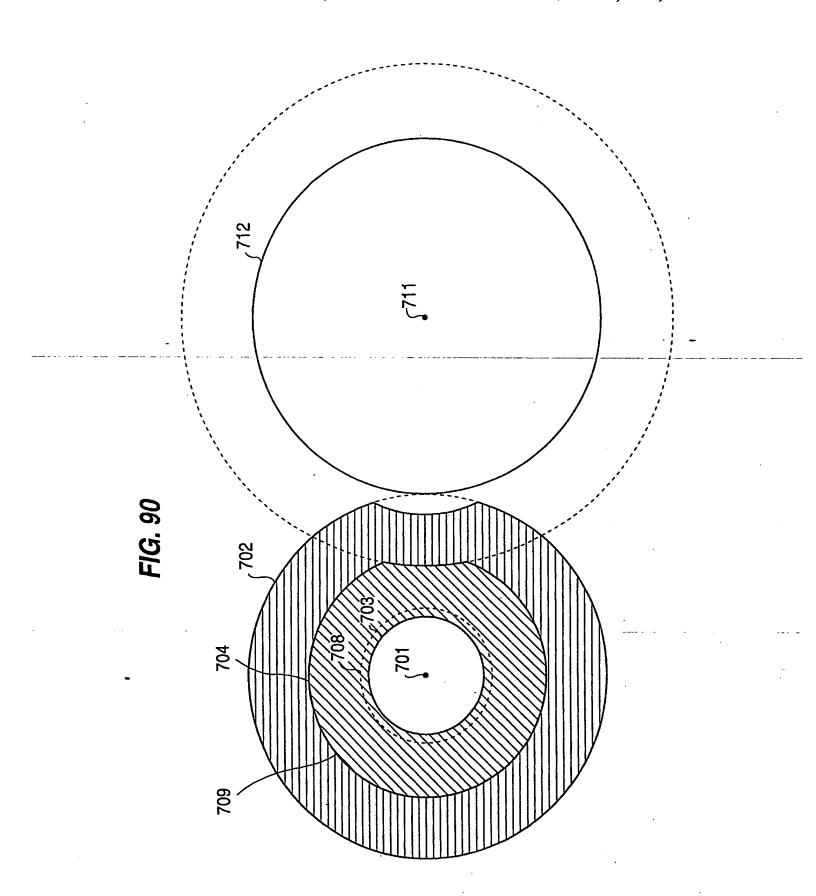


FIG. 89



Feb. 4, 1997



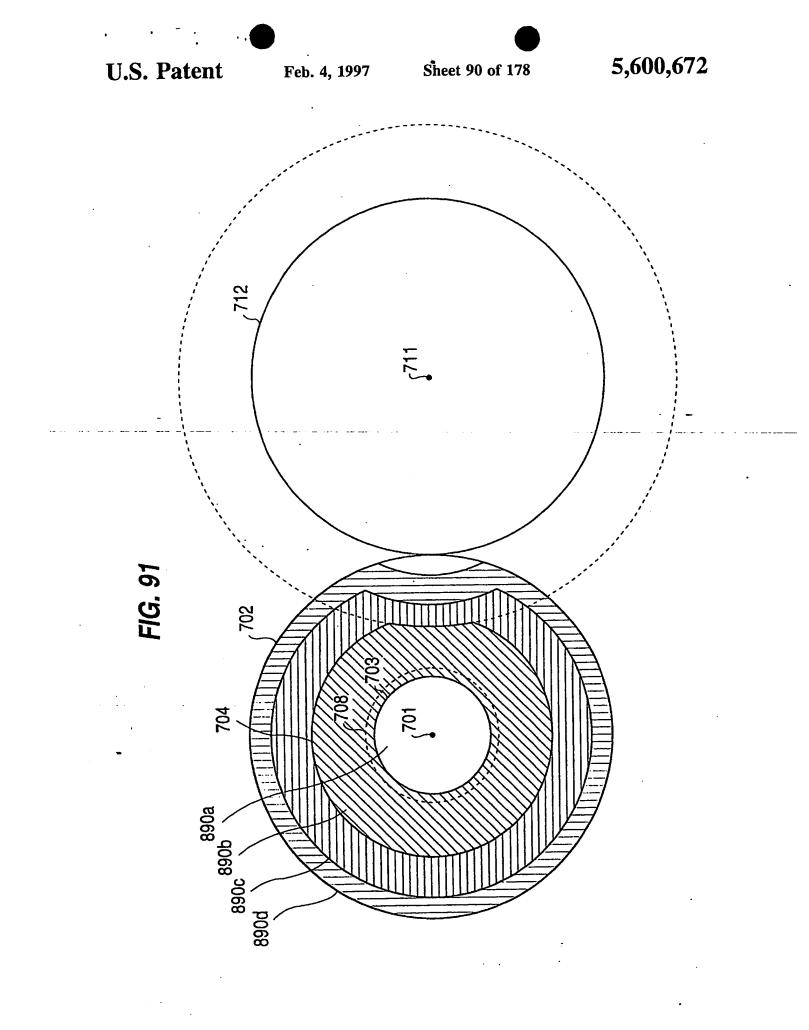
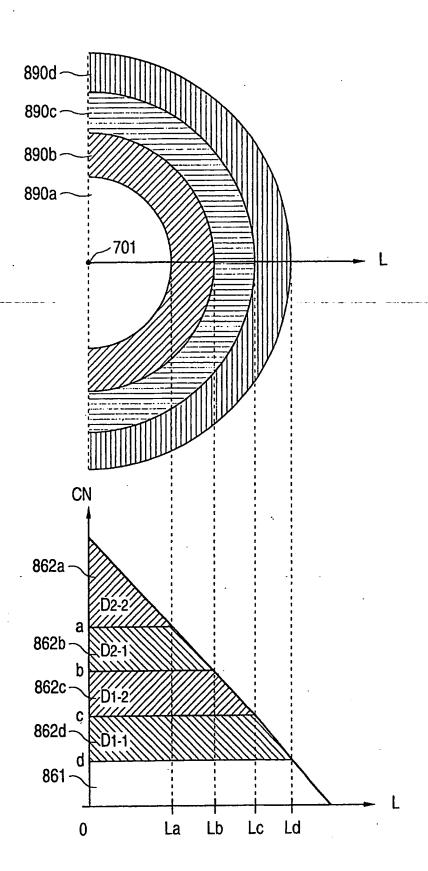
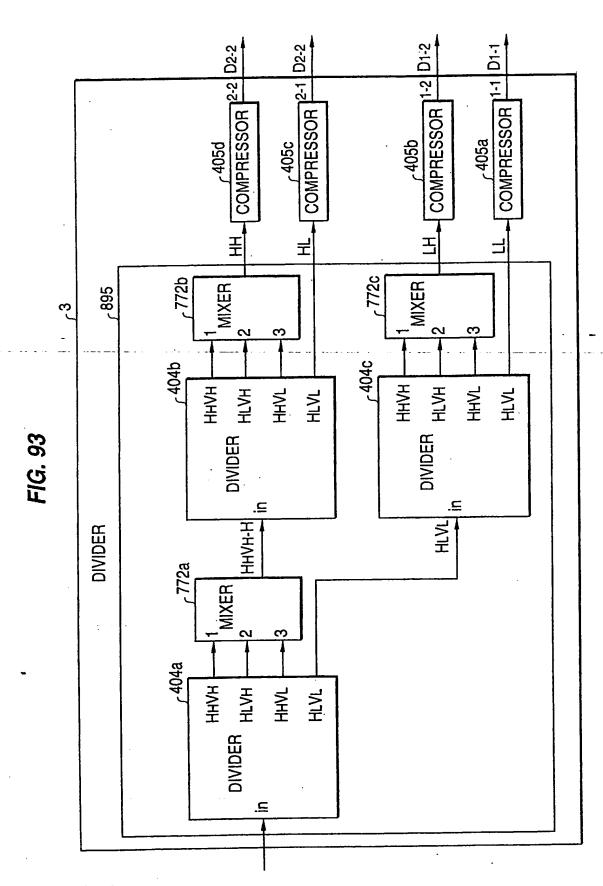


FIG. 92





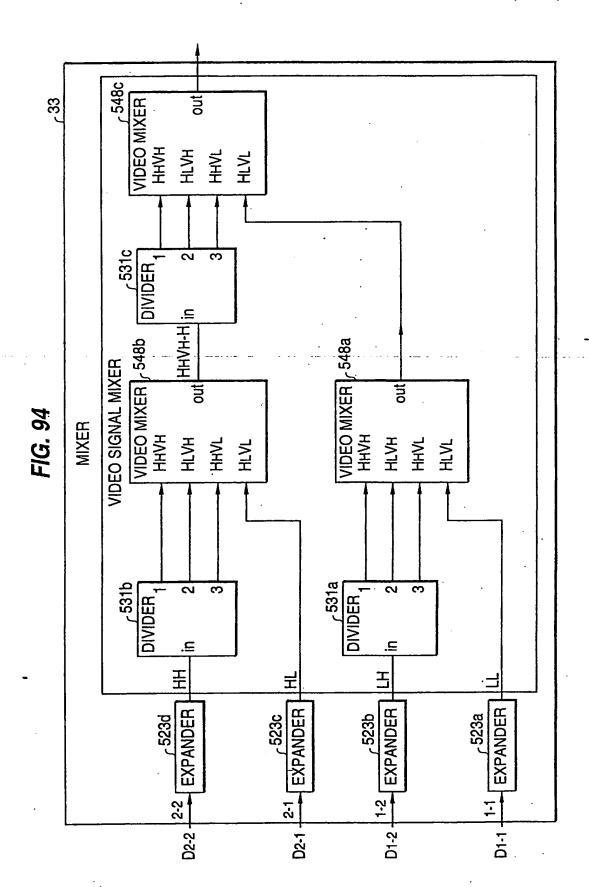
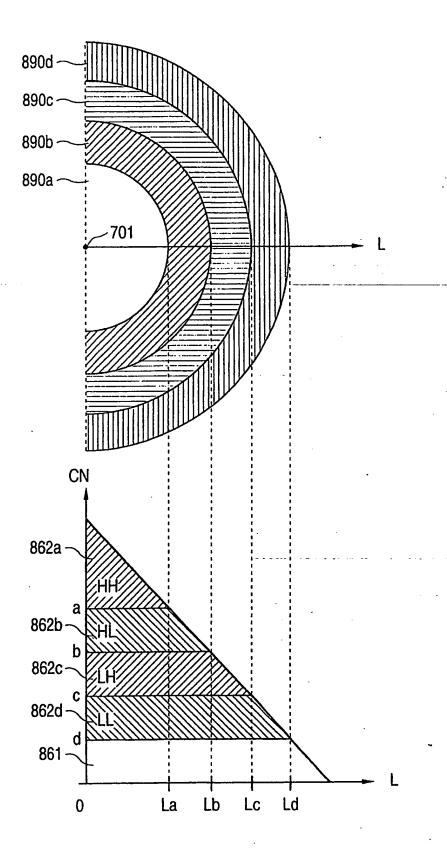
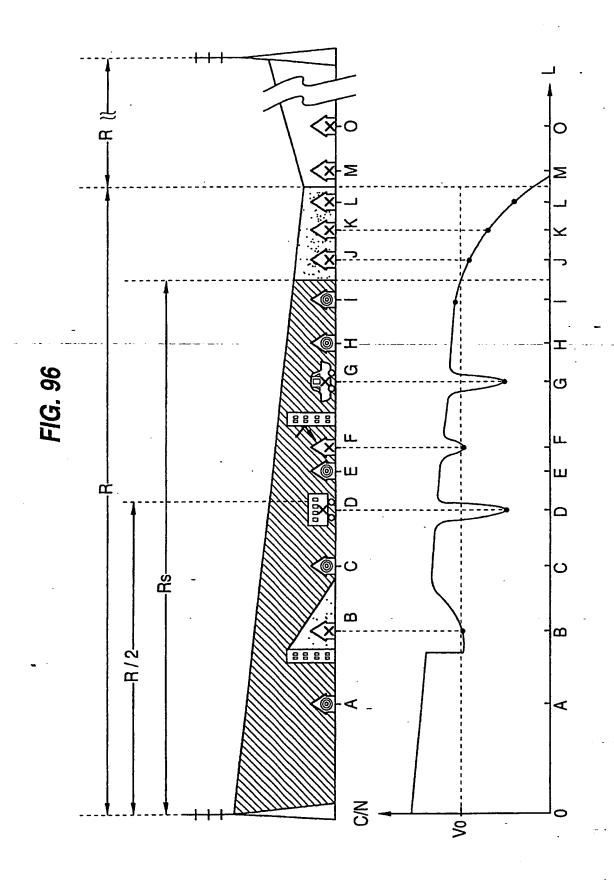


FIG. 95





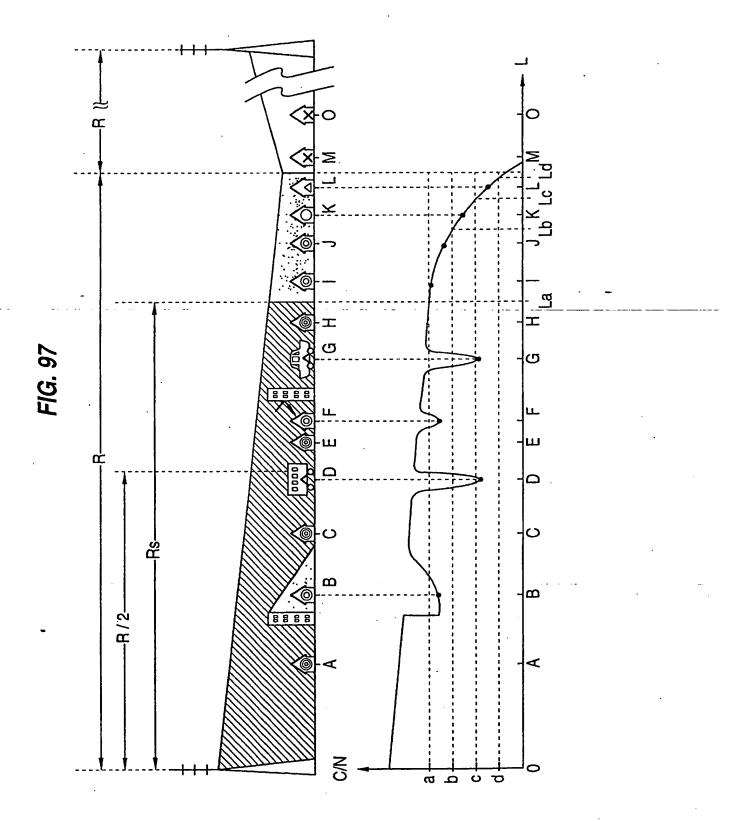


FIG. 98

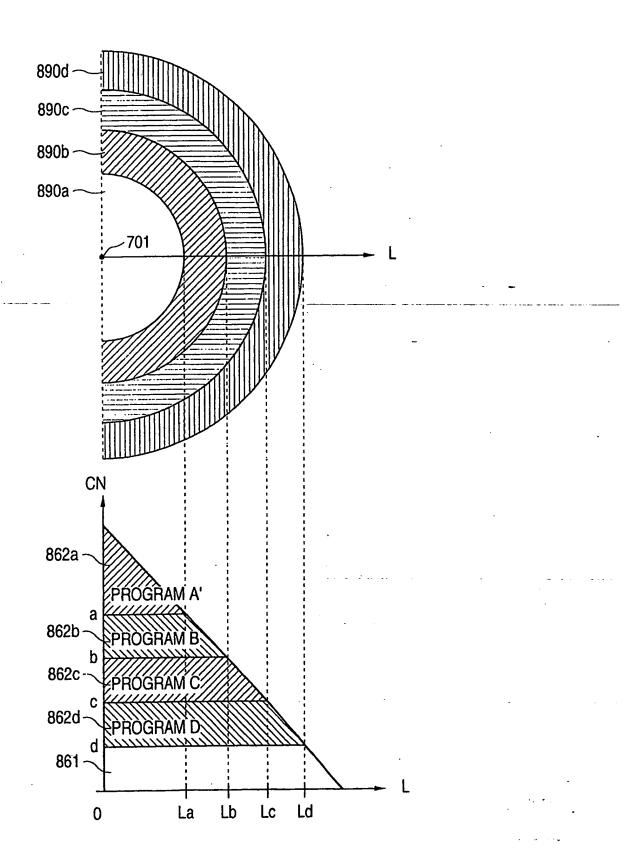


FIG. 99

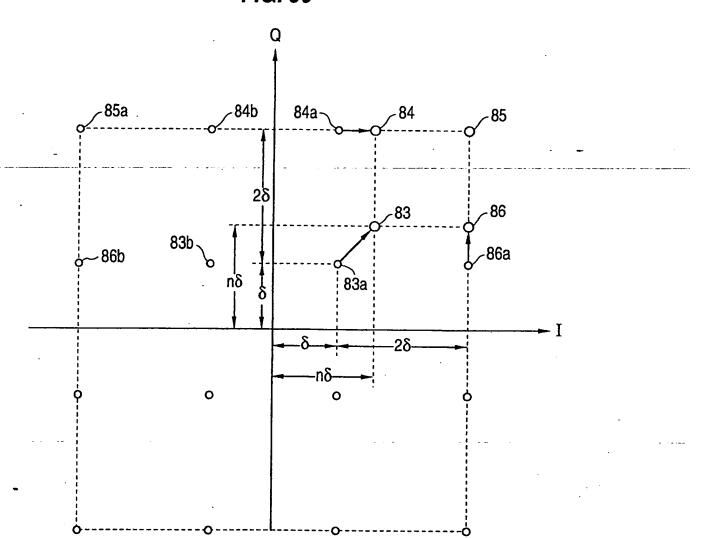


FIG. 100

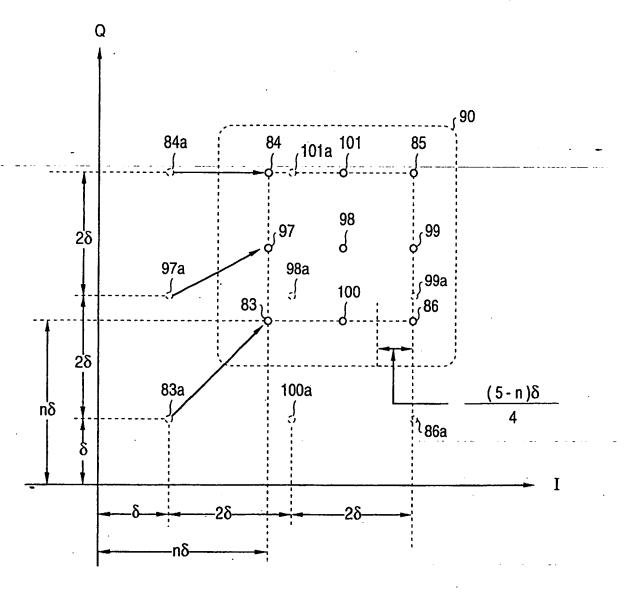


FIG. 101

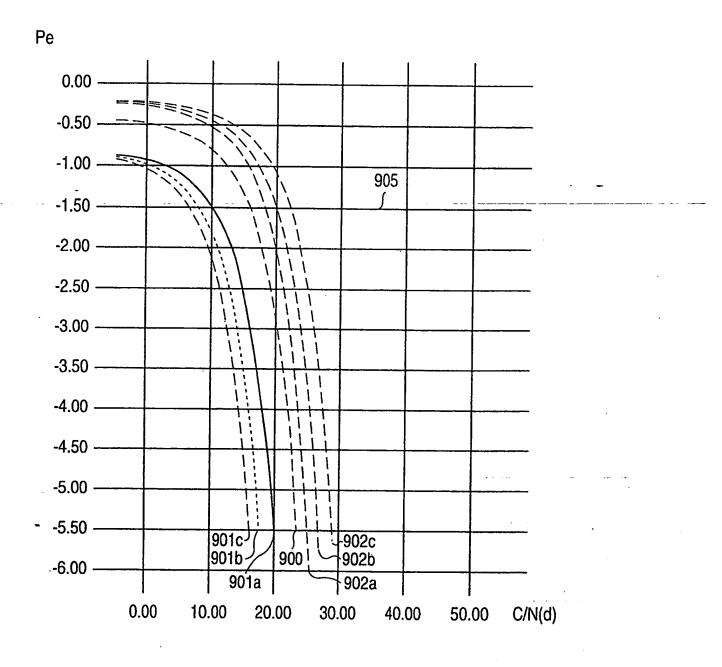


FIG. 102

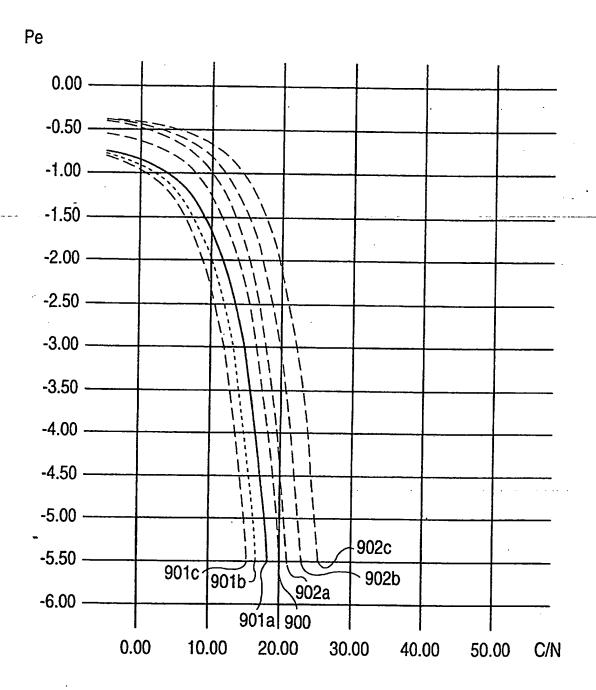


FIG. 103

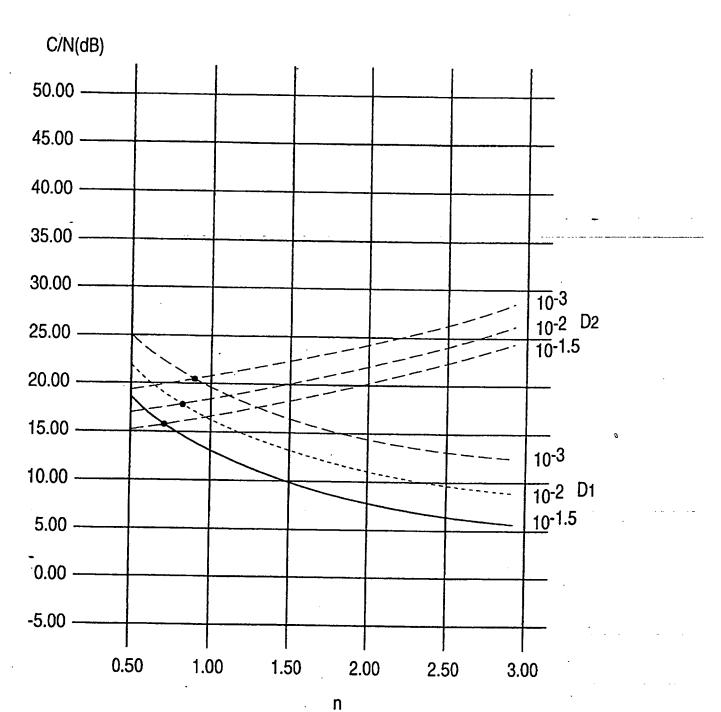
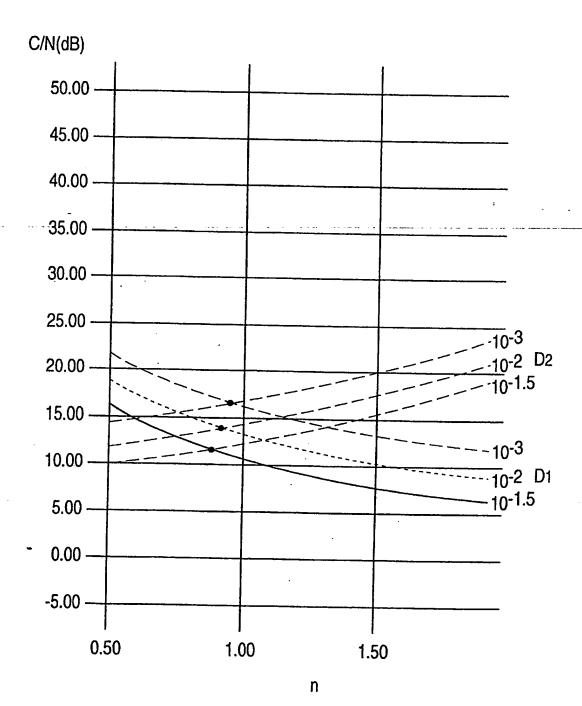
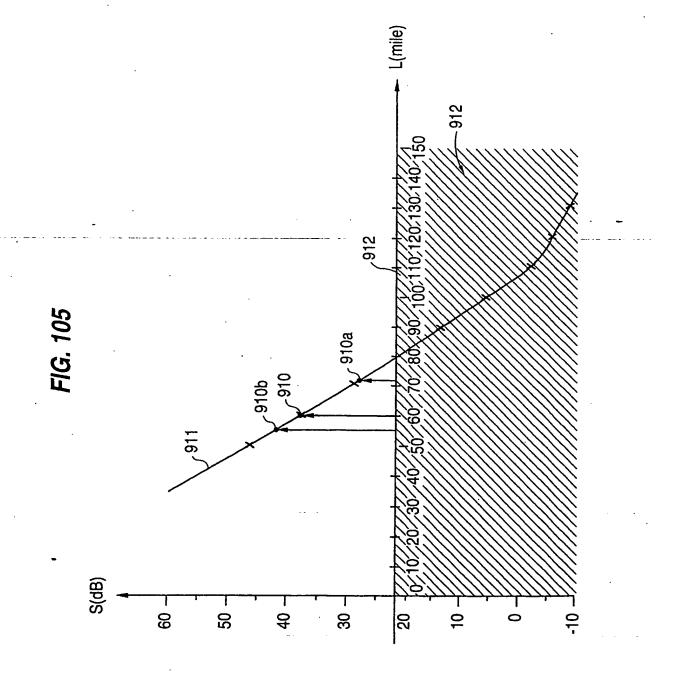
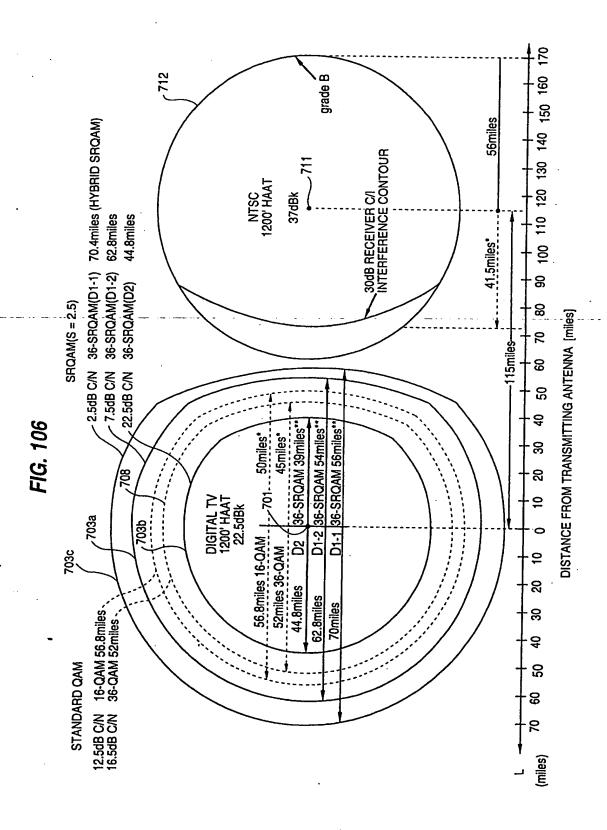
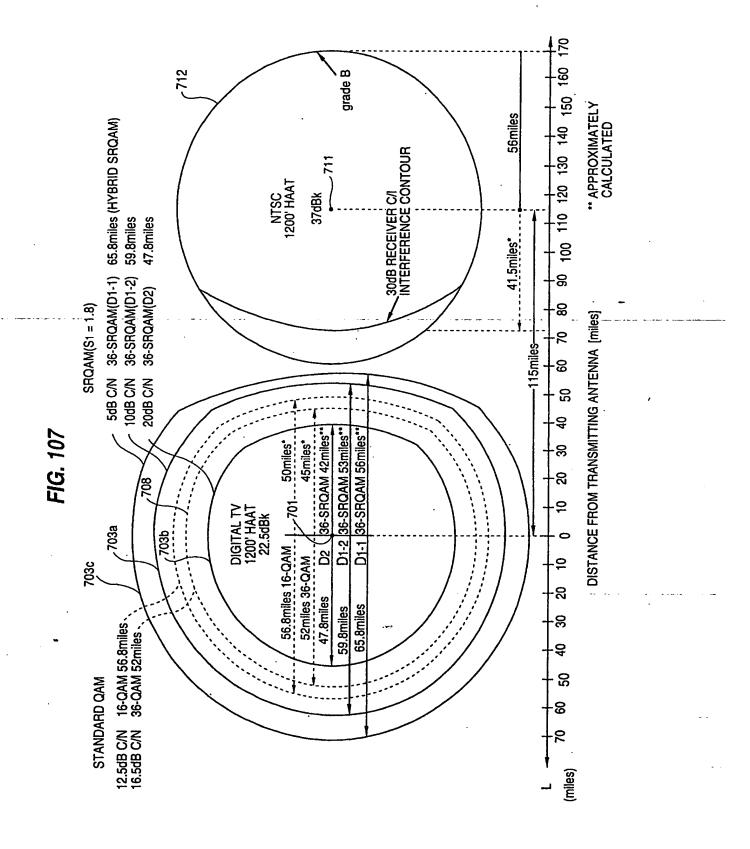


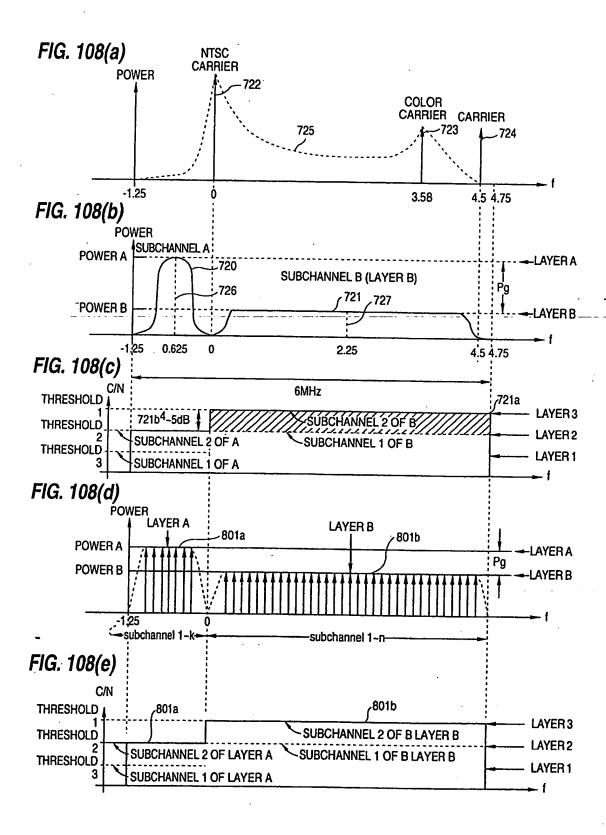
FIG. 104

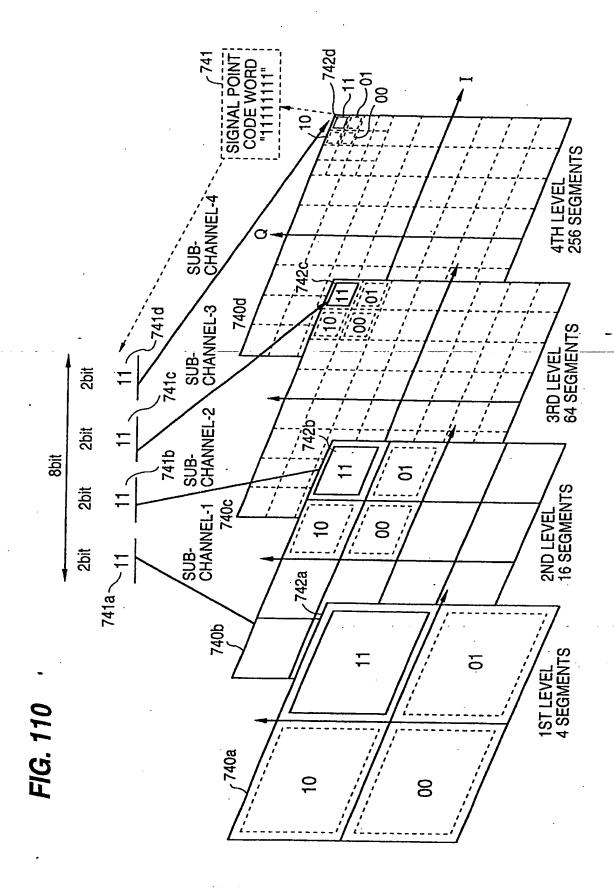












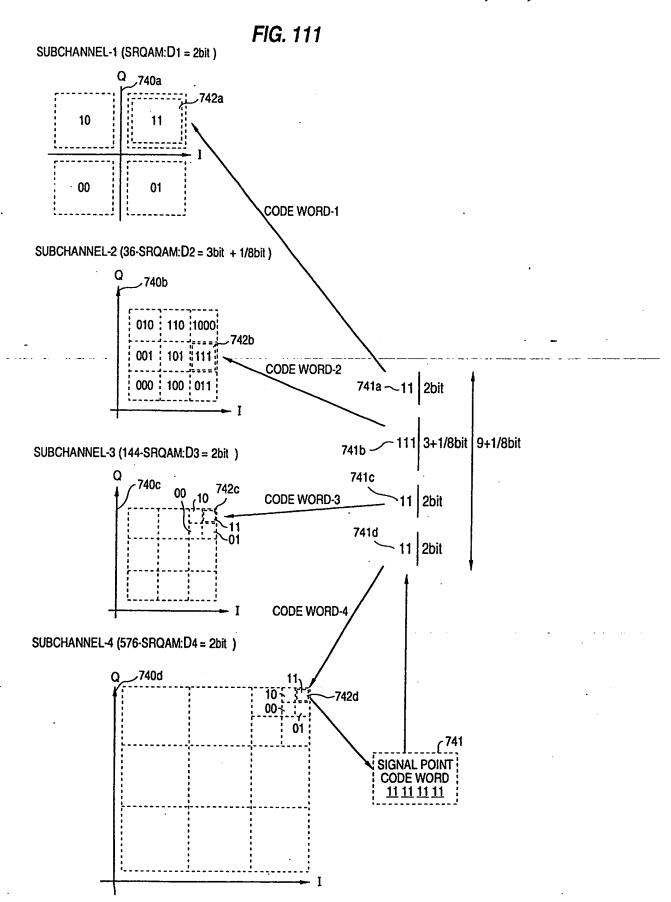
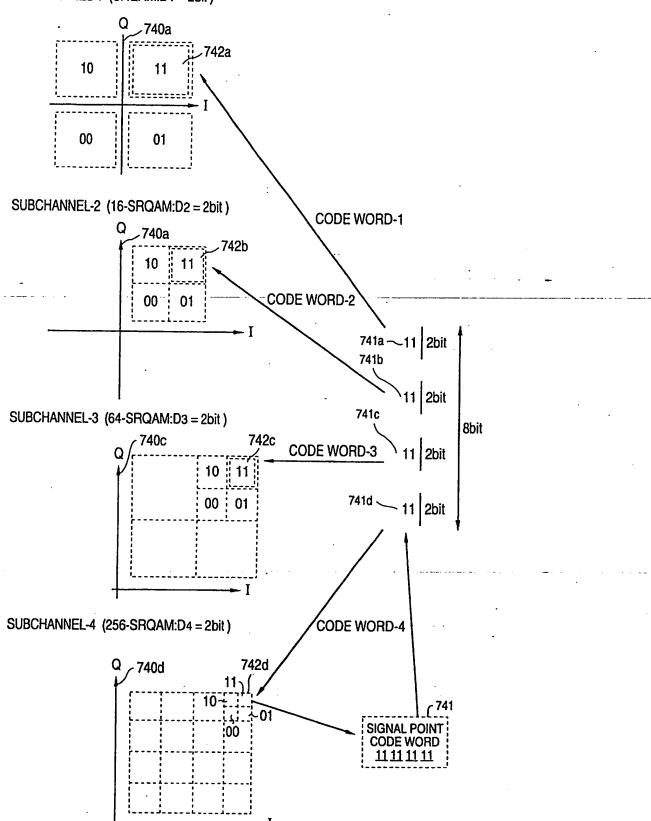
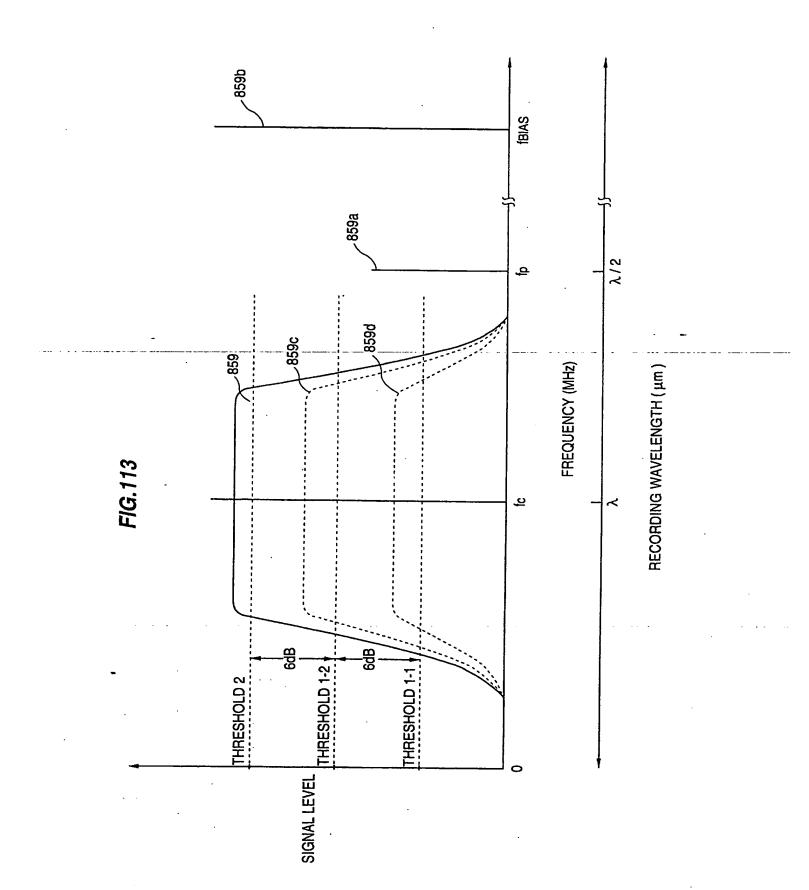
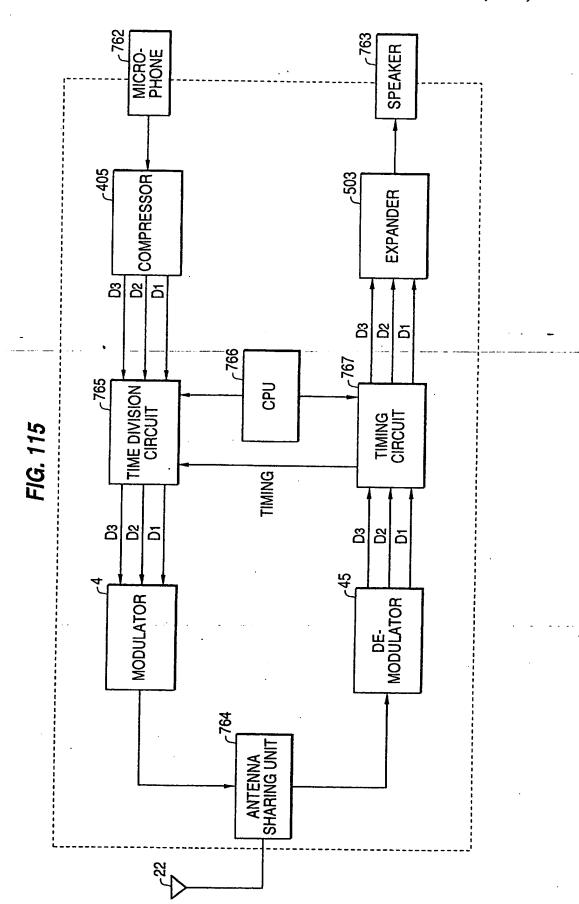


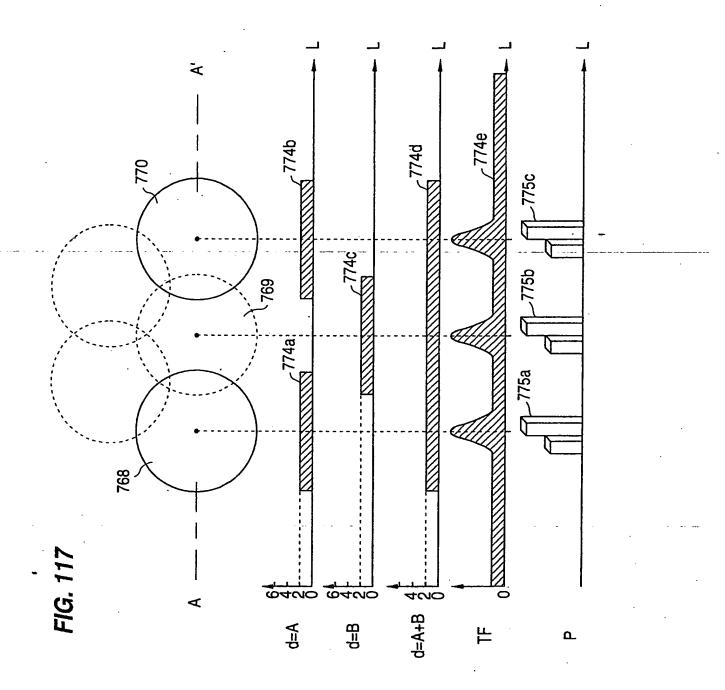
FIG. 112

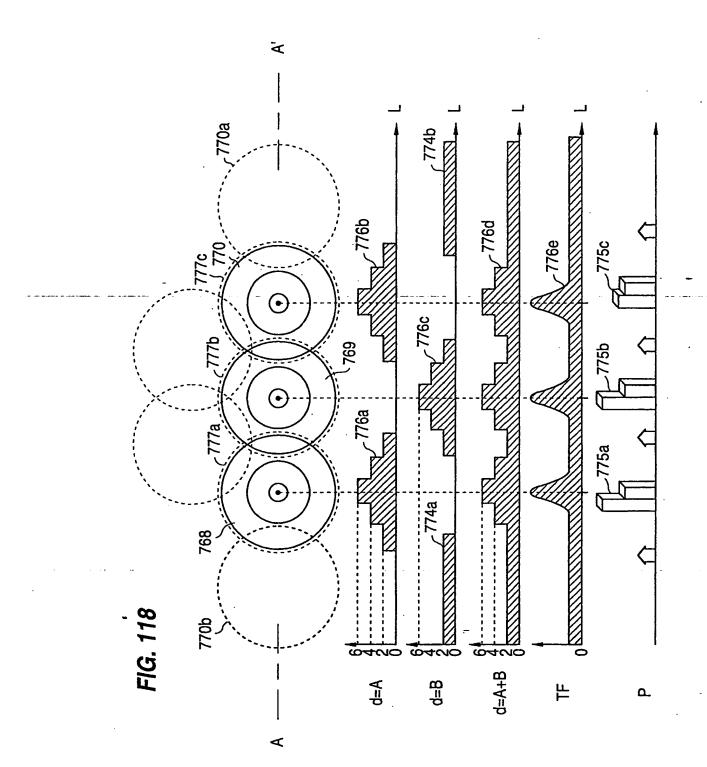
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



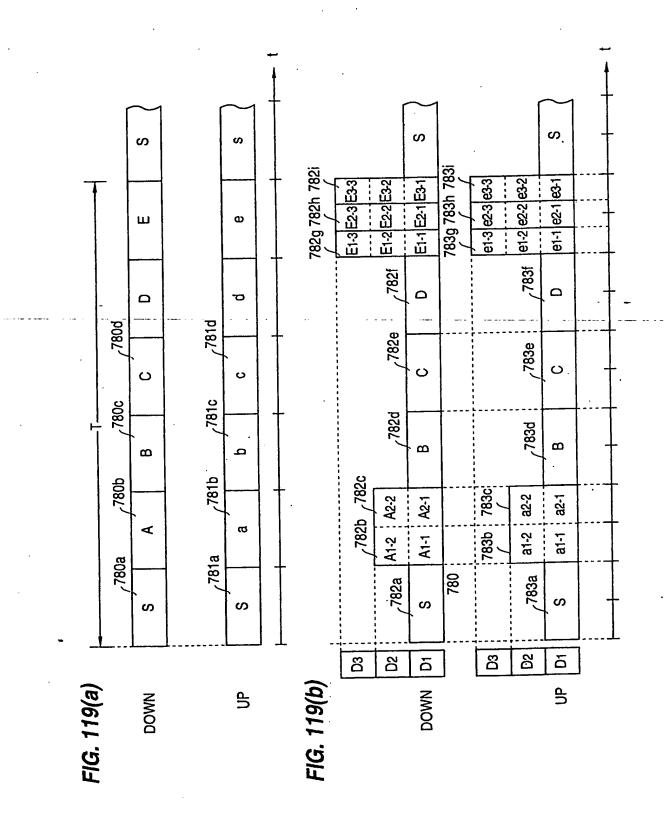


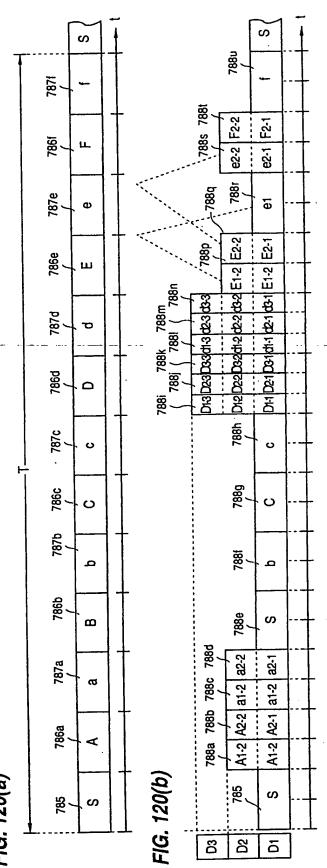


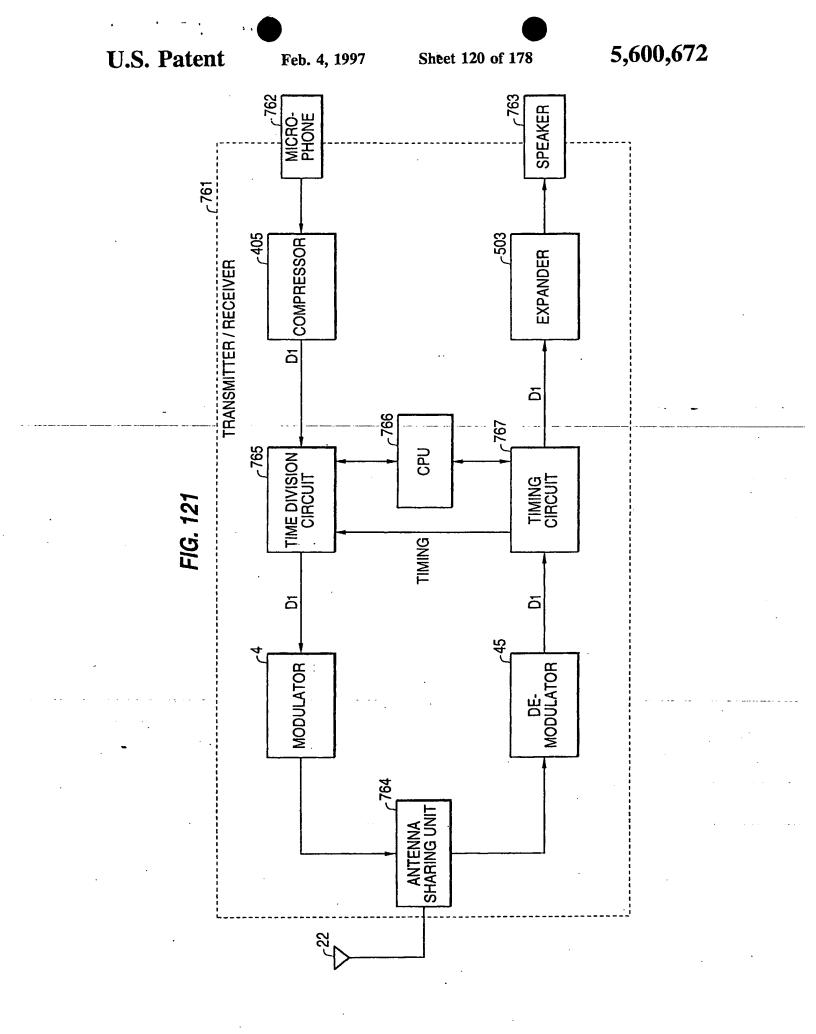


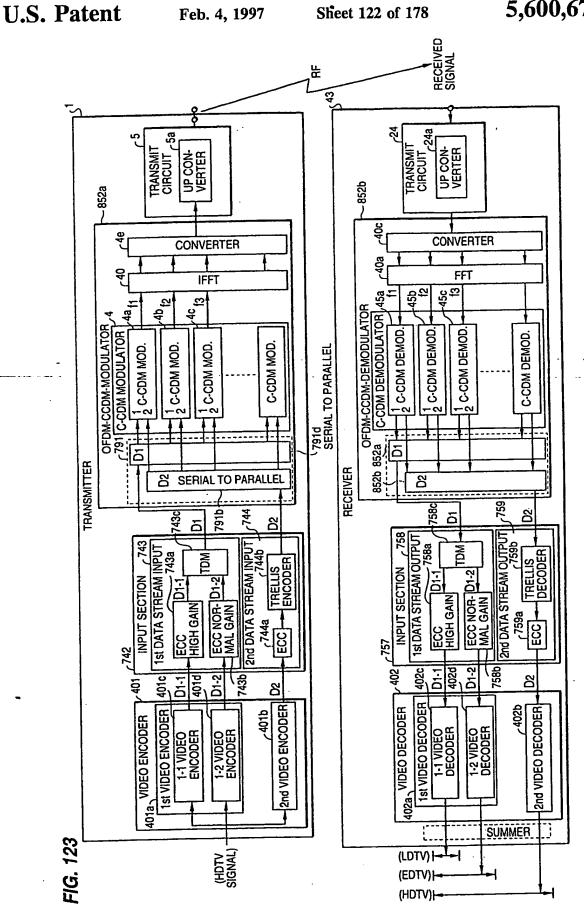


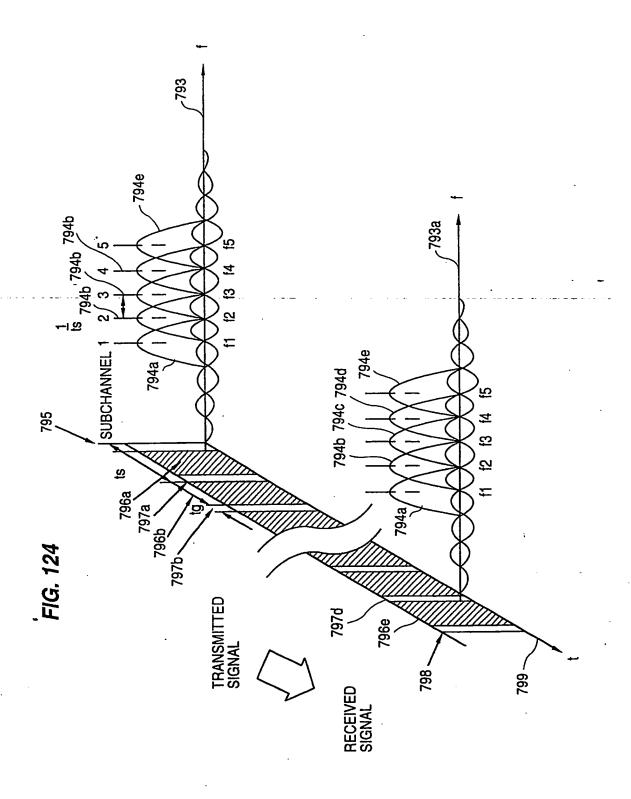
U.S. Patent

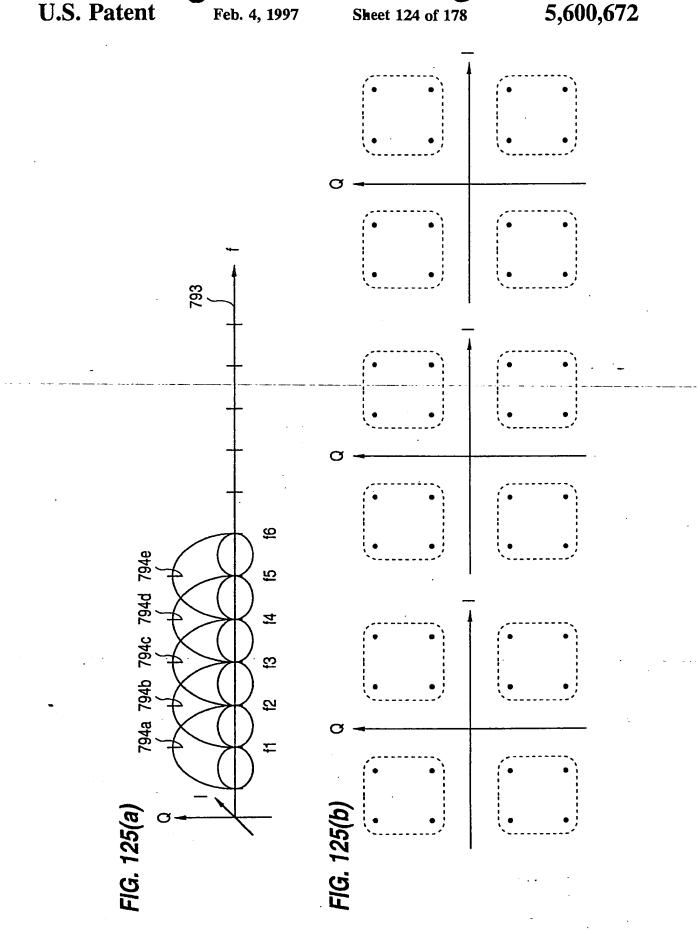


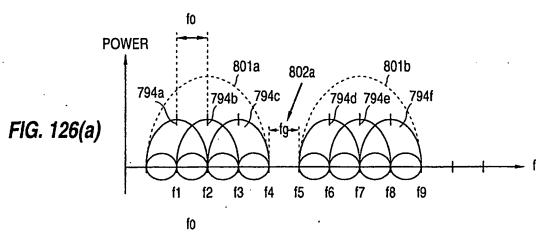


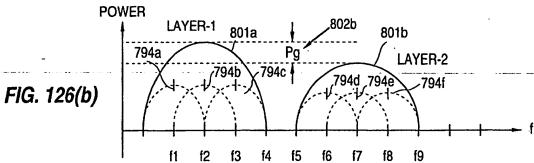


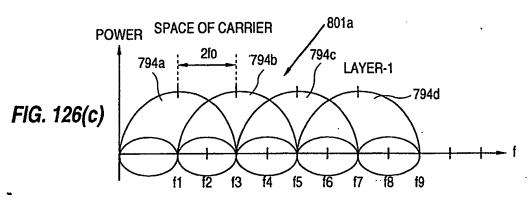


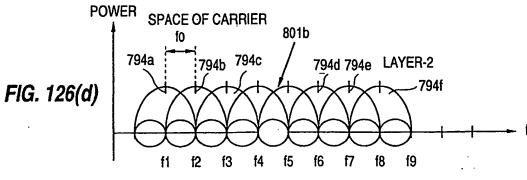












.24a ↑ RECEIVED SIGNAL 胎 43 UP CONVERTER DOWN CONVERTER INPUT CIRCUIT 852a -852b **DIVIDER SUMMER 45** .45c C-CDM MODULATOR C-CDM DEMODULATOR MODULATOR DEMODULATOR C-CDM MOD. C-CDM MOD. C-CDM DEMOD. с-сом ремор. C-CDM DEMOD. с-срм мор. с-срм мор. TRANSMITTER RECEIVER SERIAL TO PARALLEL CONVERTER PARALLEL TO SERIAL CONVERTER 758c 758 759 Σ IST DATA STREAM INPUT 1St DATA STREAM OUTPUT 2nd DATA STREAM INPU **OUTPUT SECTION** 2nd DATA STREAM OU ECC NOR- D1-2 MAL GAIN INPUT SECTION ECC NOR- D1-MAL GAIN ECC HIGH GAIN ECC HIGH GAIN 401a 402d 401c 401d 743b 402a 2nd VIDEO ENCODER 1st VIDEO DECODER 1st VIDEO ENCODER 2nd VIDEO DECODER VIDEO ENCODER VIDEO DECODER 1-1 VIDEO ENCODER 1-2 VIDEO ENCODER 1-2 VIDEO DECODER 1-1 VIDEO DECODER (LDTV) |- 1-1 (EDTV) |-(HDTV)⊢

FIG. 12

FIG. 128(a)

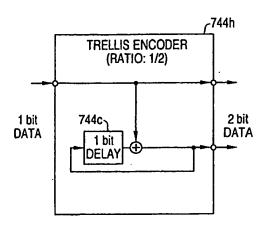


FIG. 128(d)

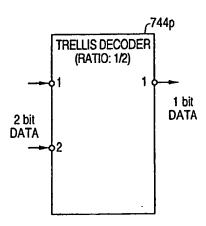


FIG. 128(b)

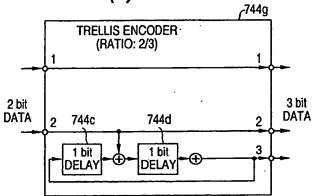


FIG. 128(e)

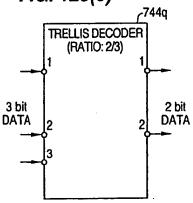


FIG. 128(c)

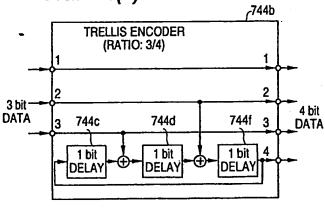
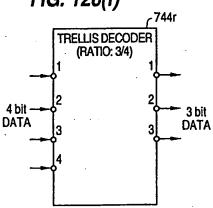
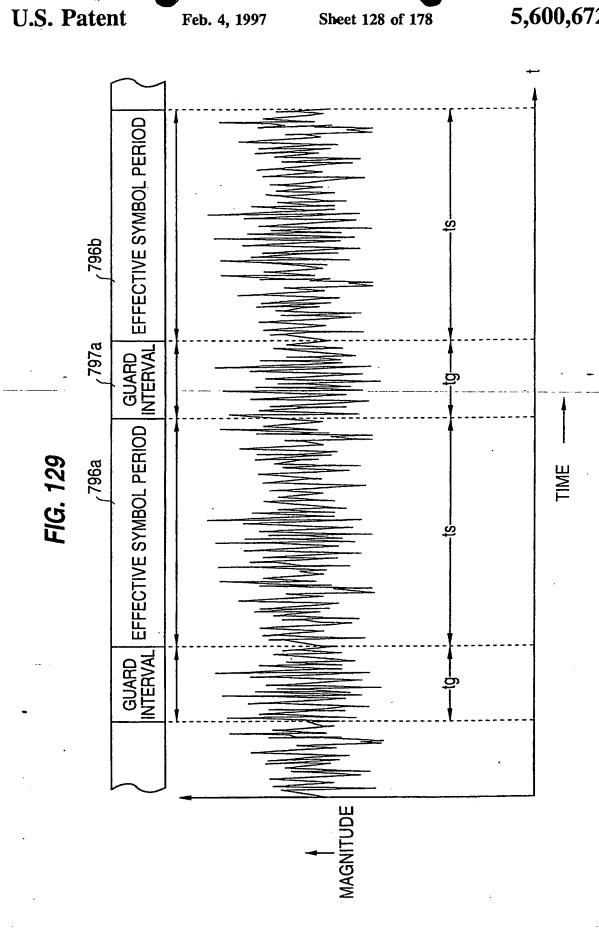
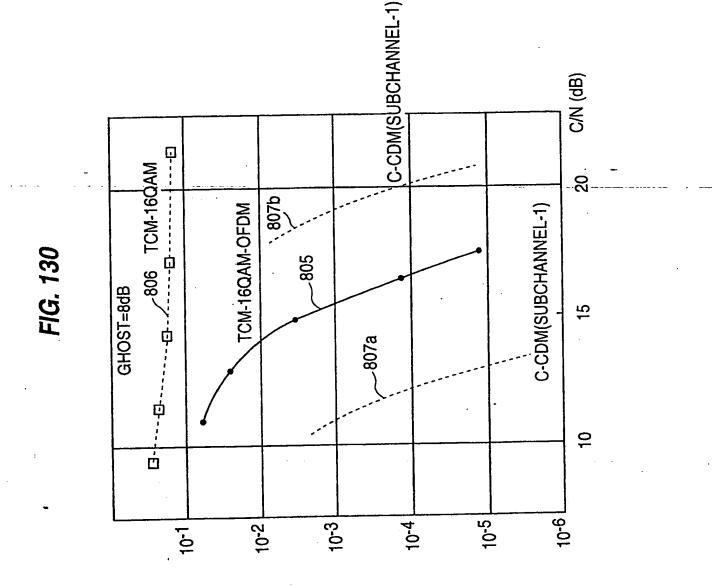
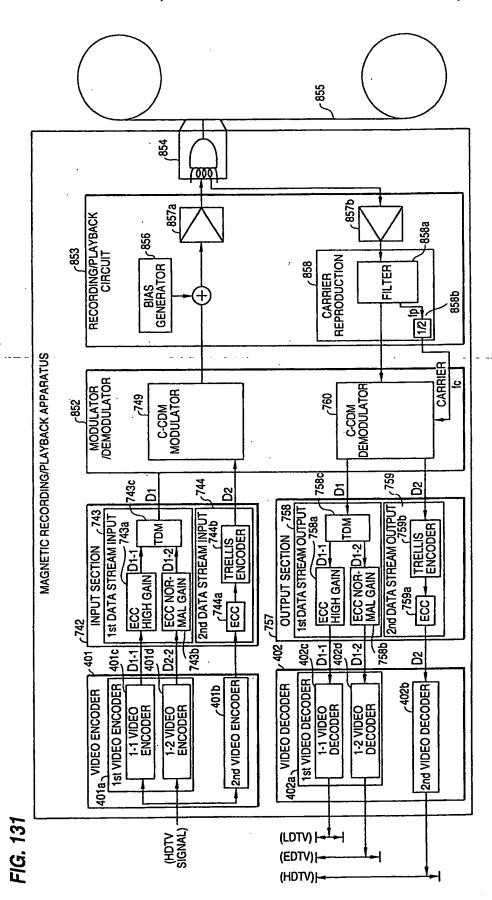


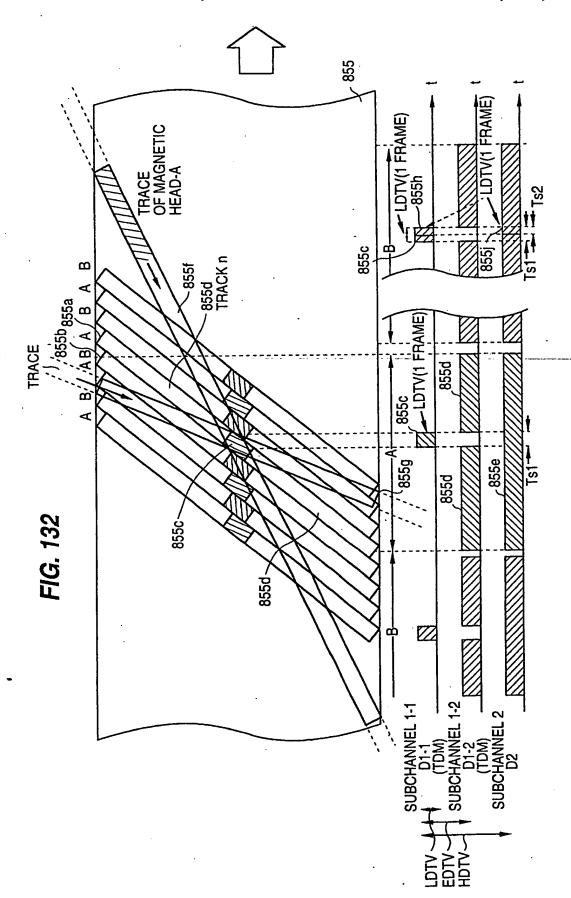
FIG. 128(f)

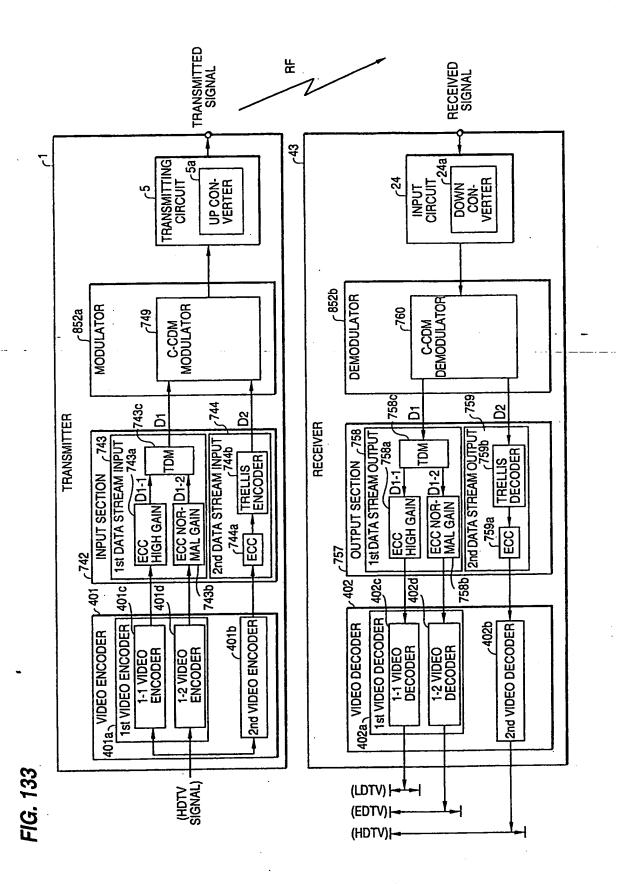




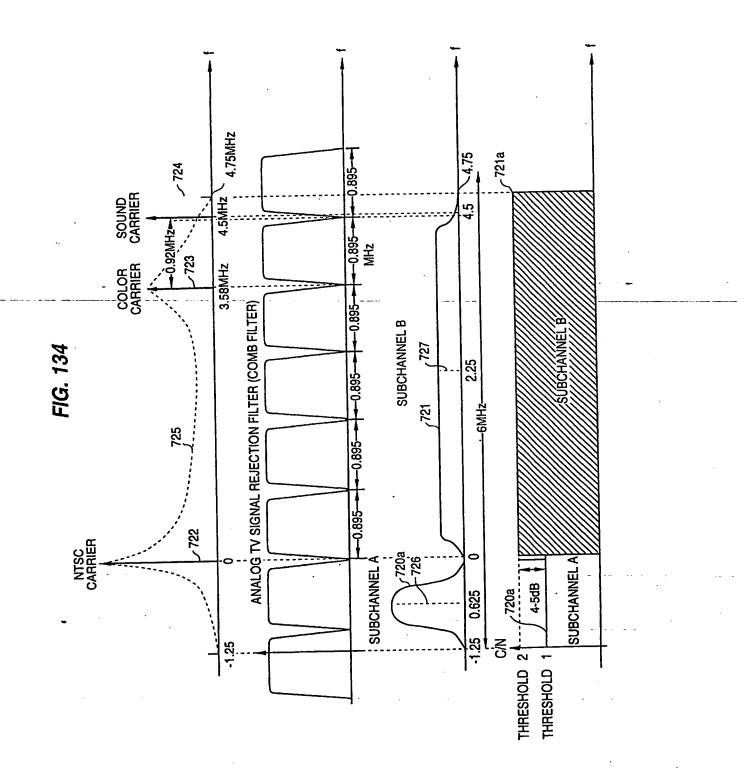




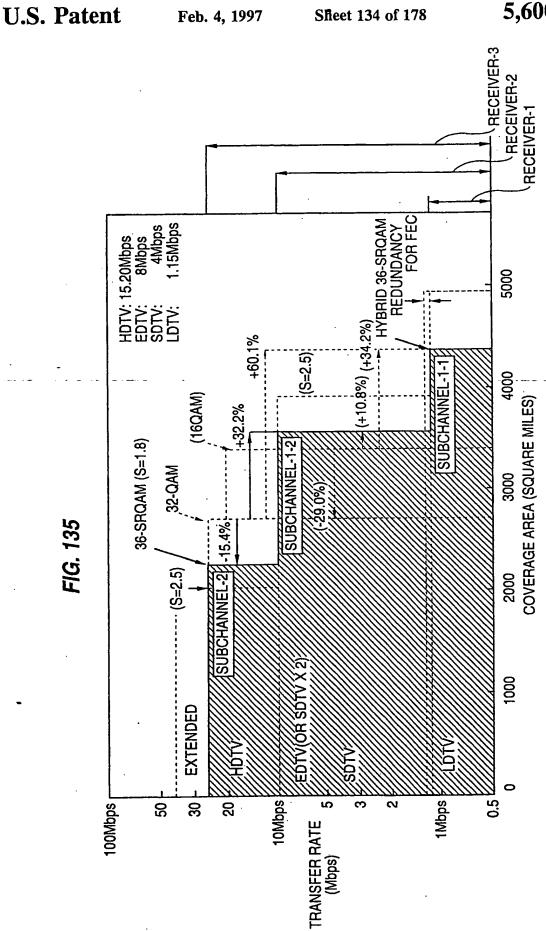




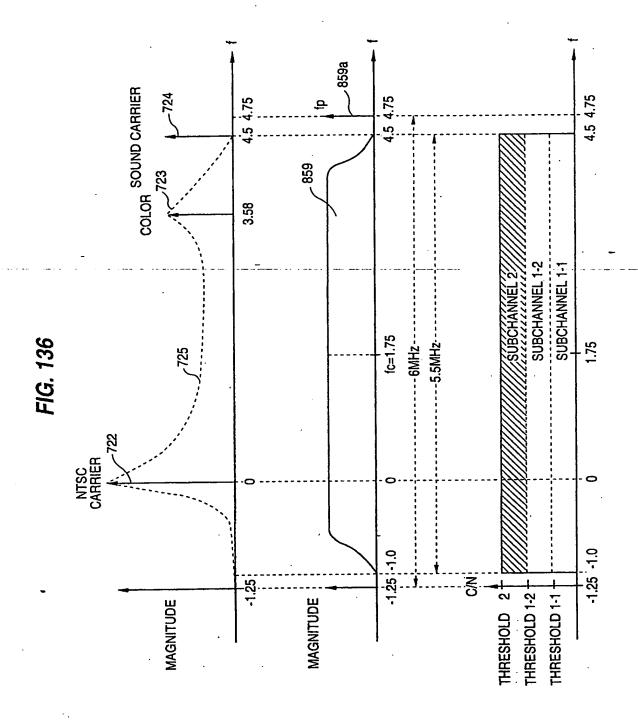
U.S. Patent

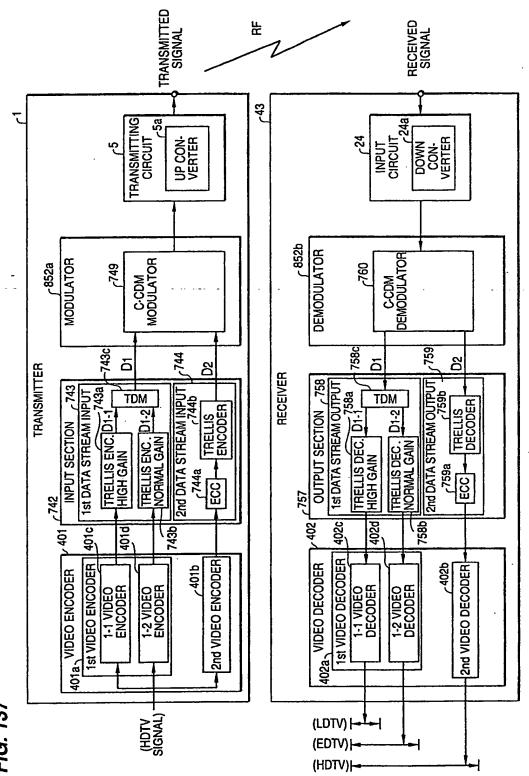






U.S. Patent





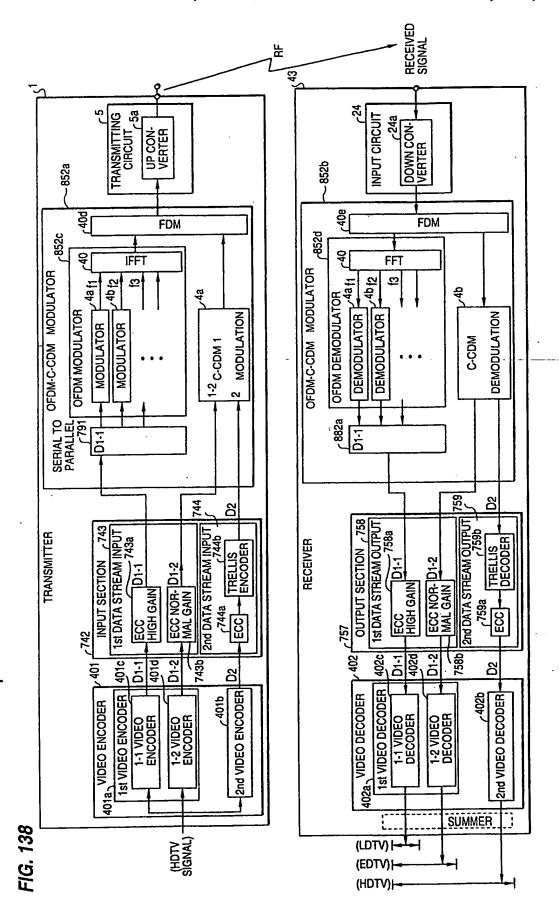


FIG. 139

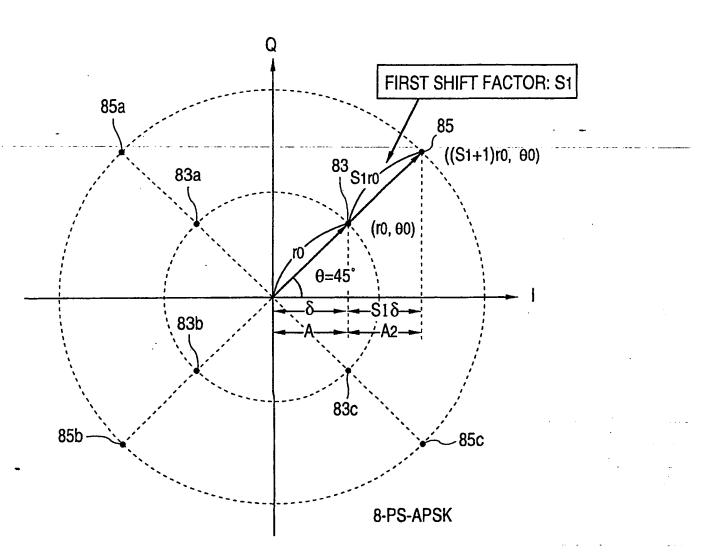


FIG. 140

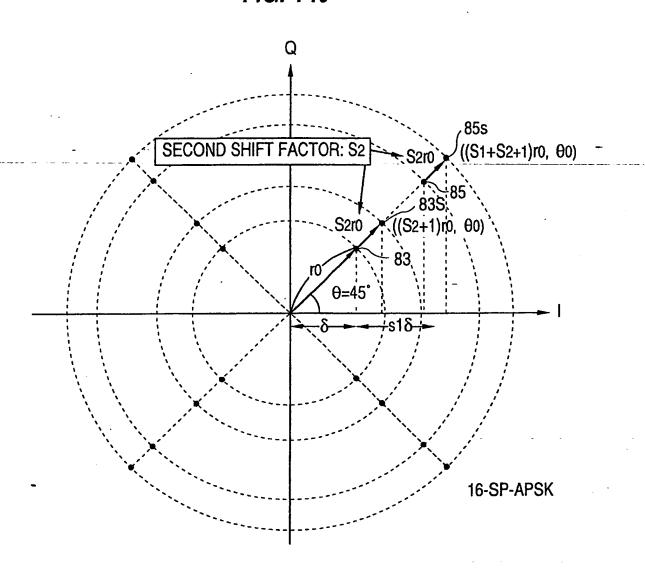


FIG. 141

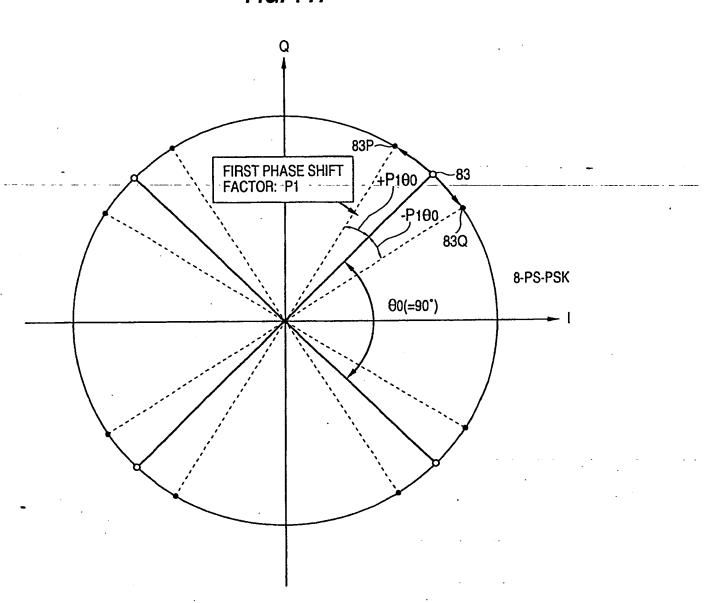
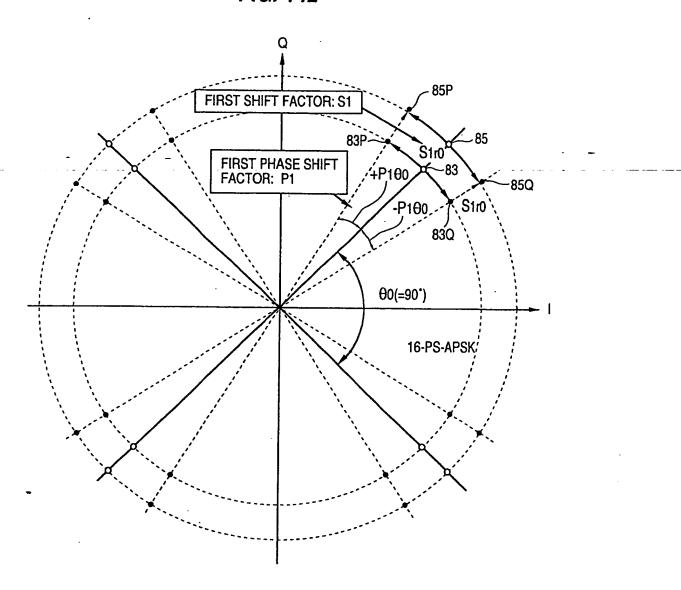
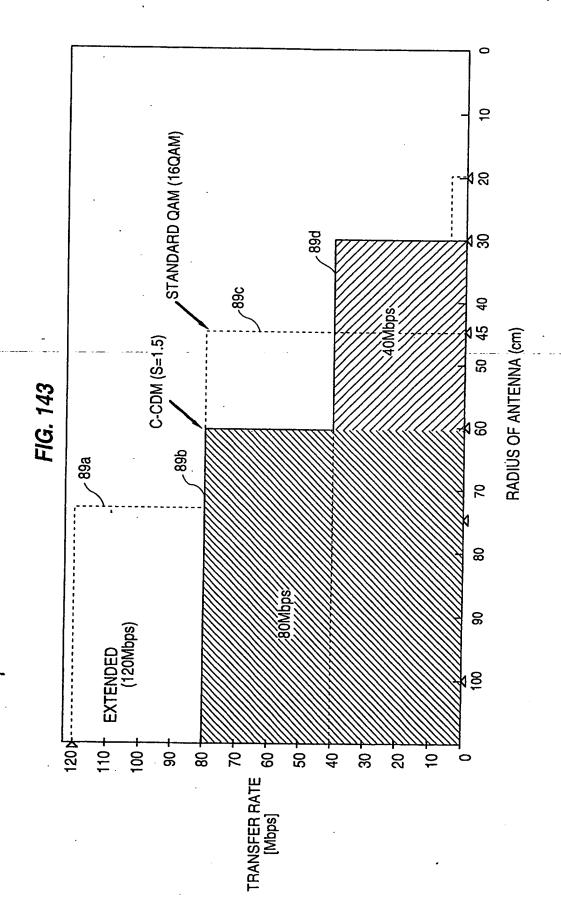


FIG. 142





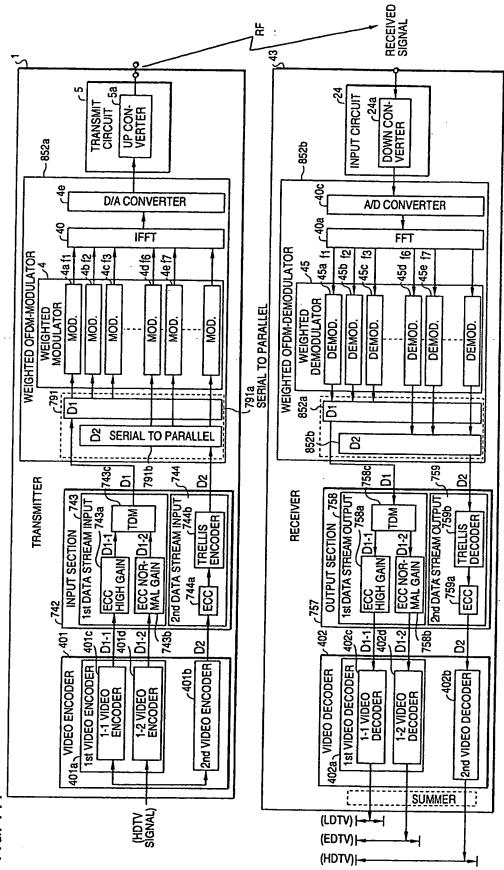


FIG. 144

FIG. 145(a)

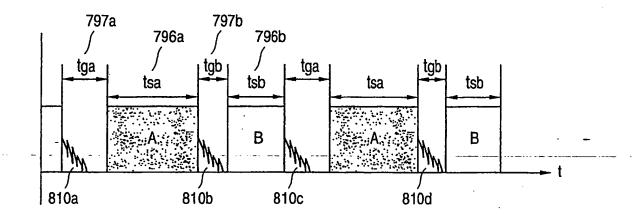
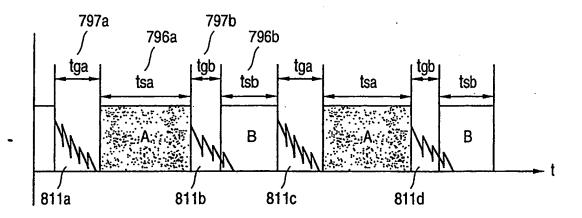
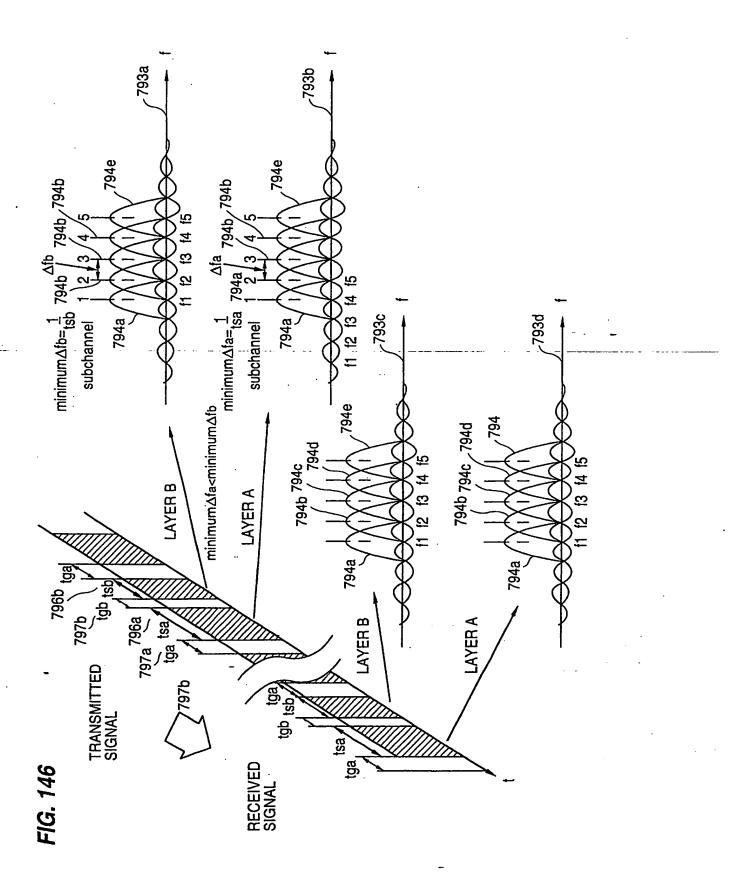
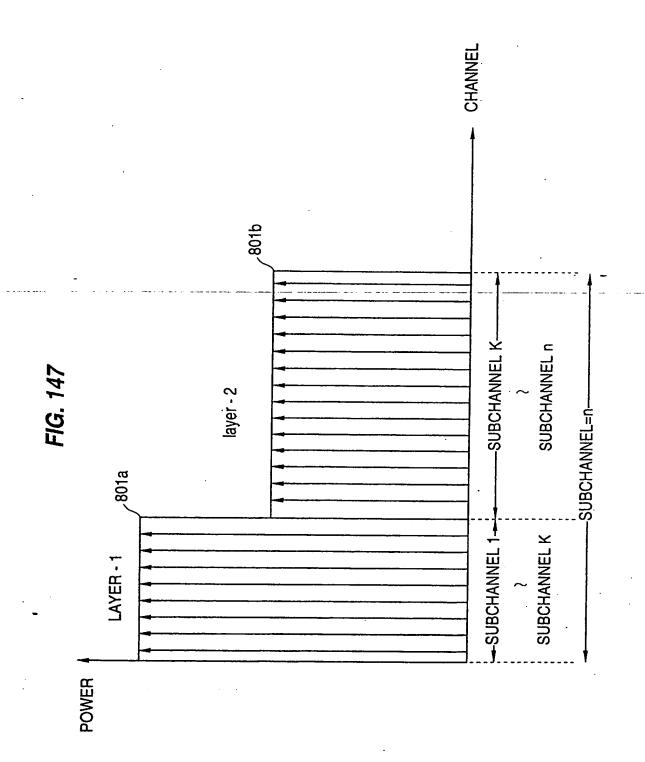
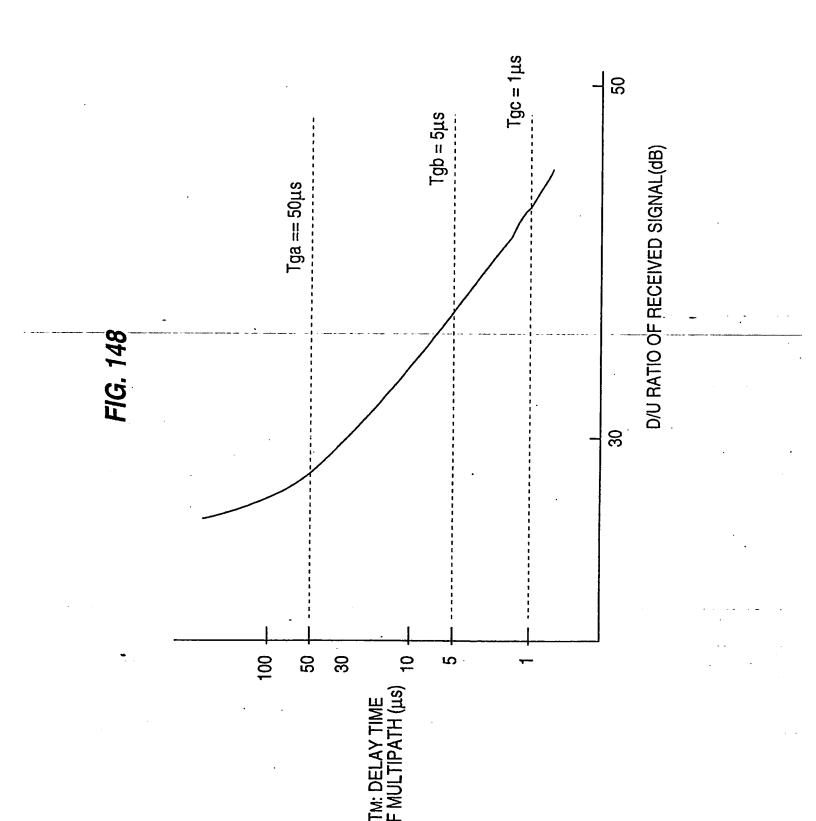


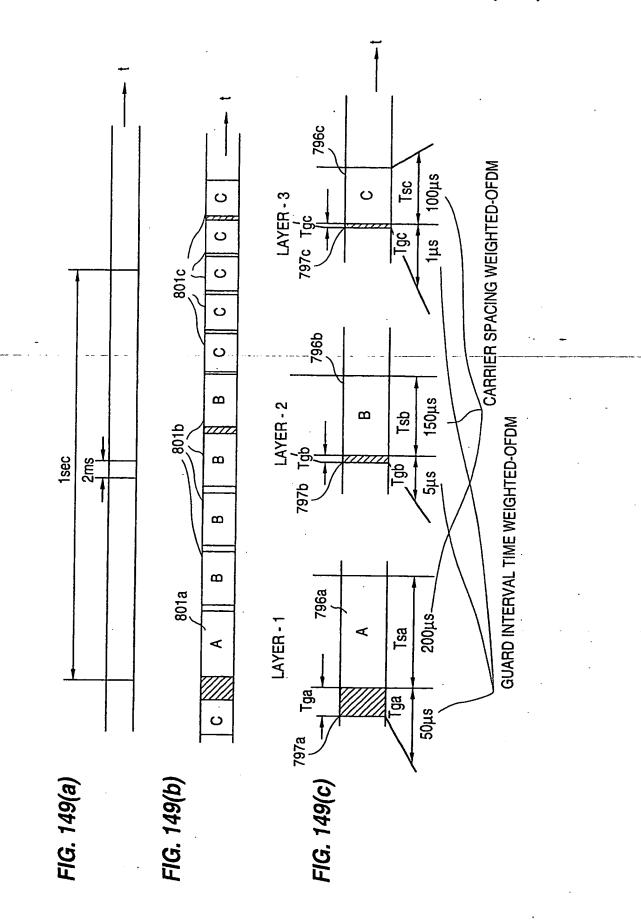
FIG. 145(b)

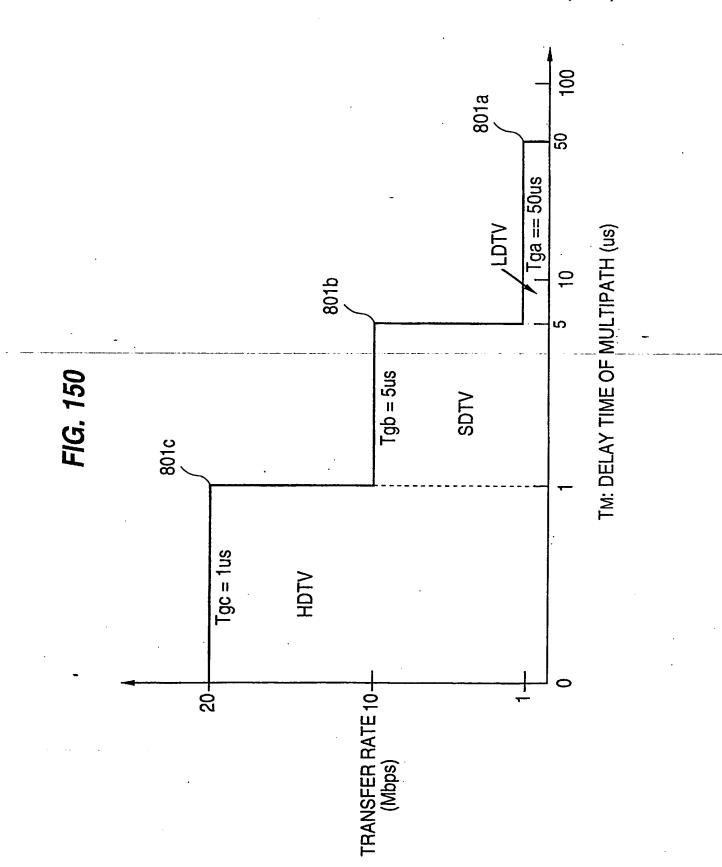


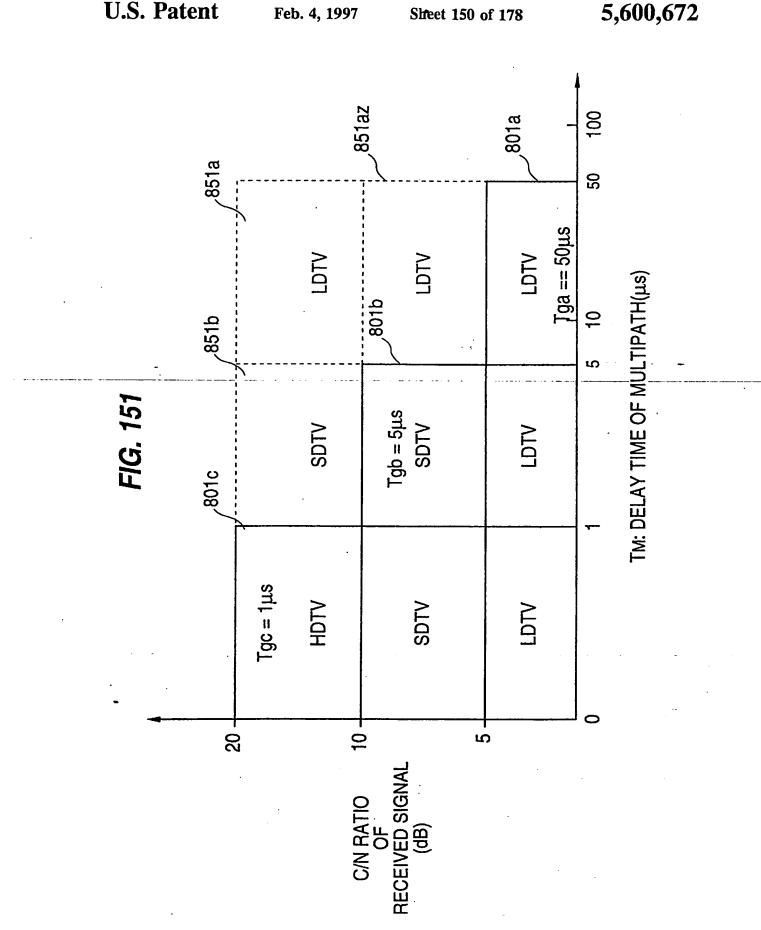


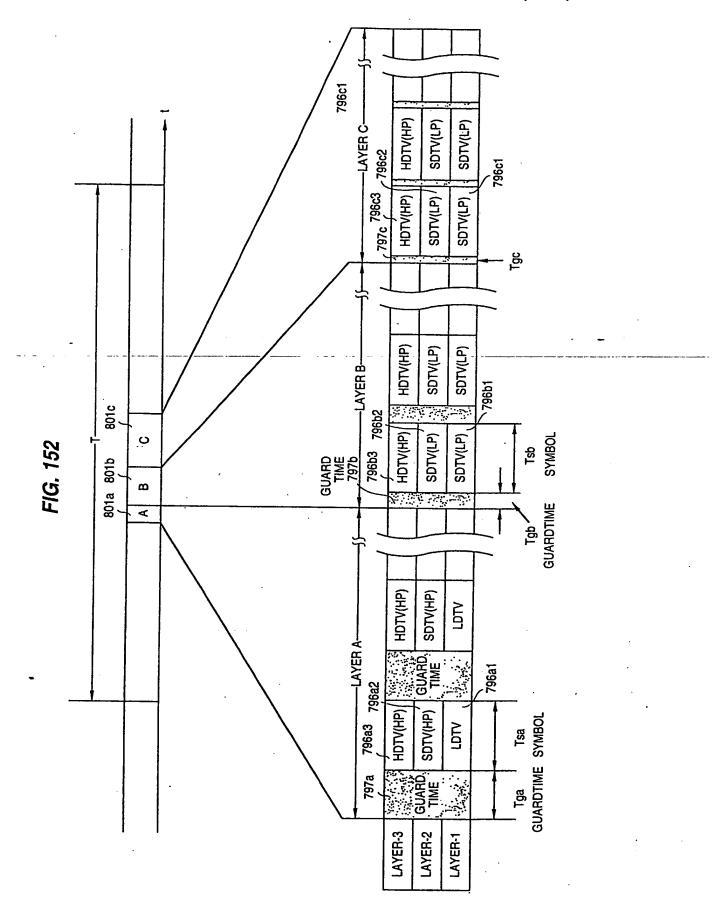




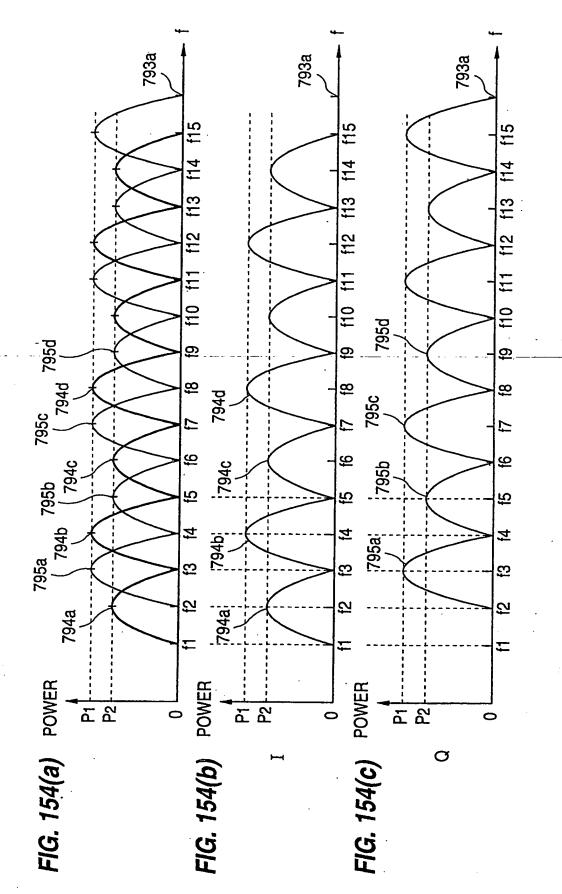








(D/U = 30dB)DELAY TIME OF MULTIPATH SIGNAL (μs) LAYER2-B -801b LAYER3-C -801c LDTV TRANSFER RATE (Mbps) FIG. 153 25 \ 전 LDTV CNR(dB) 5dB



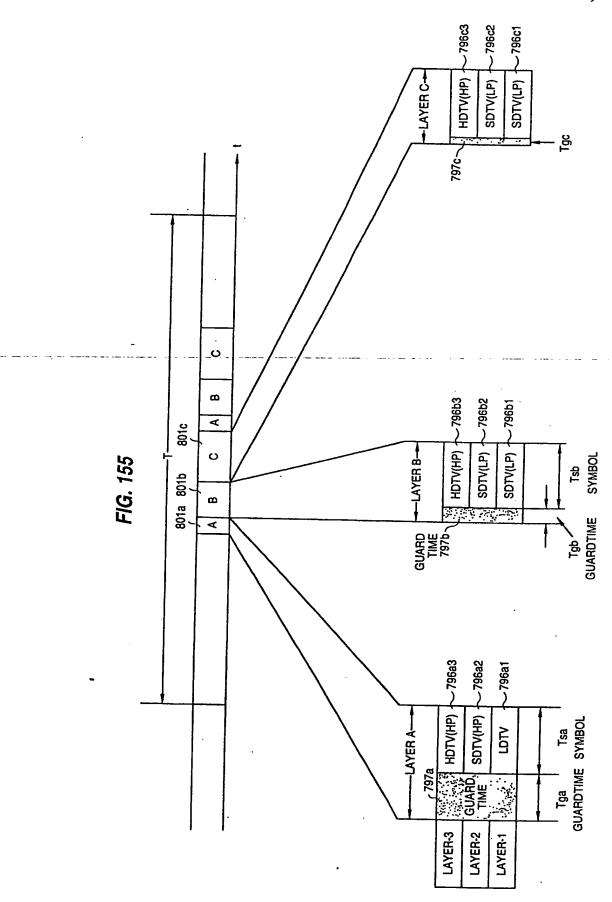
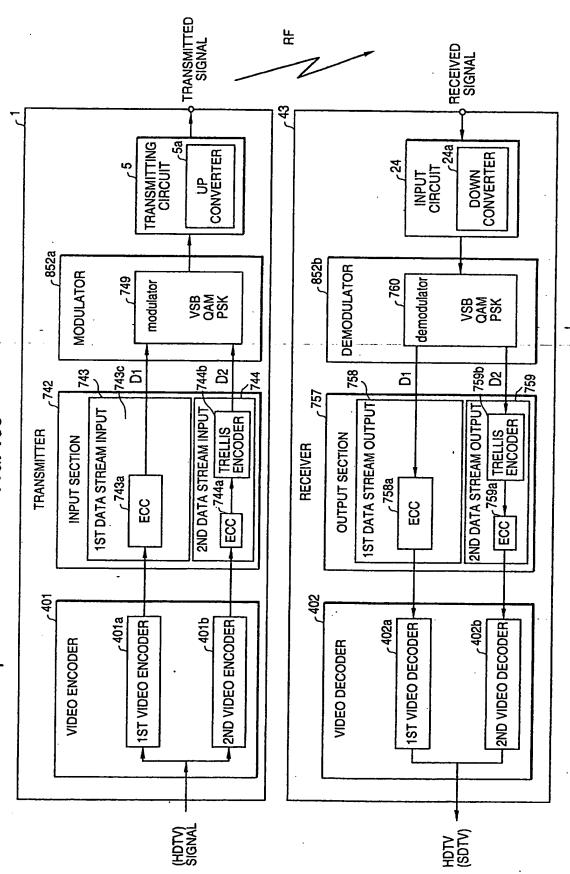
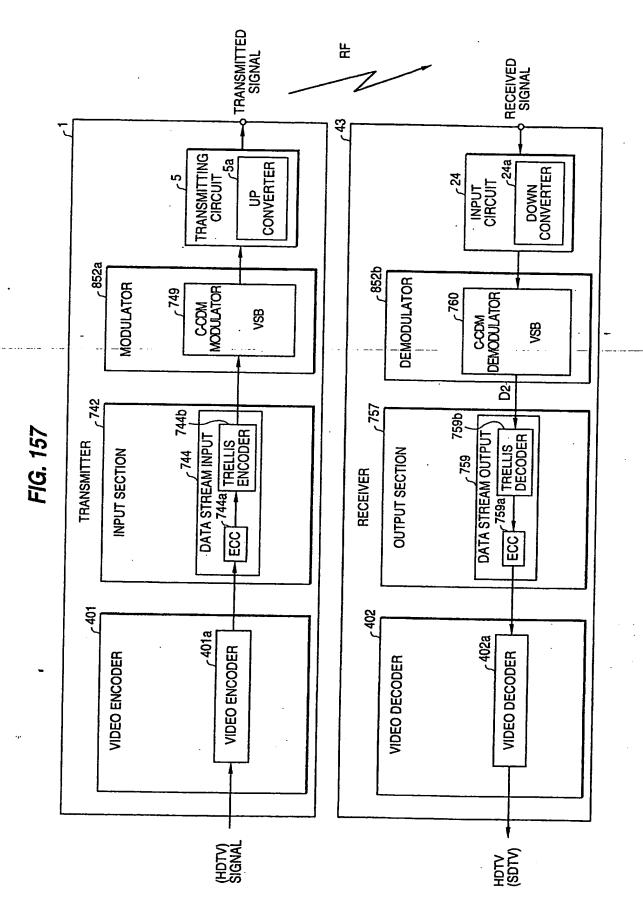


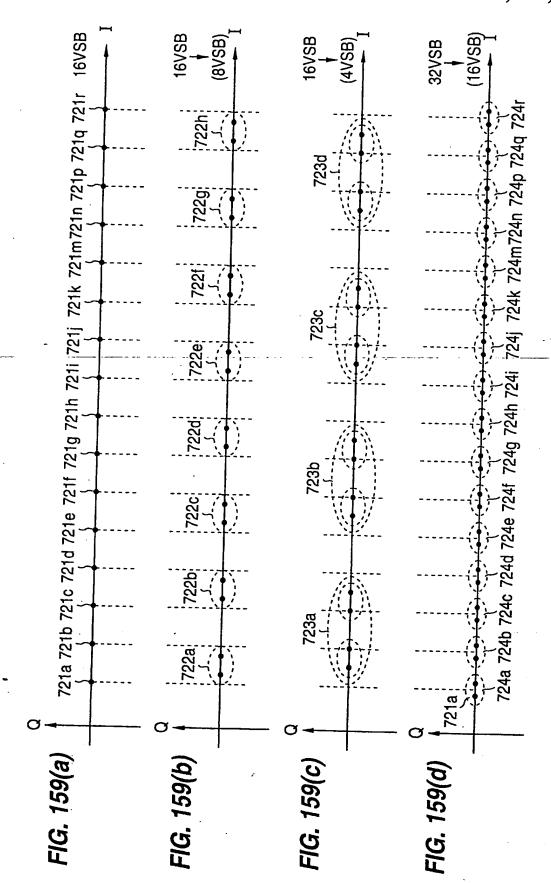
FIG. 156

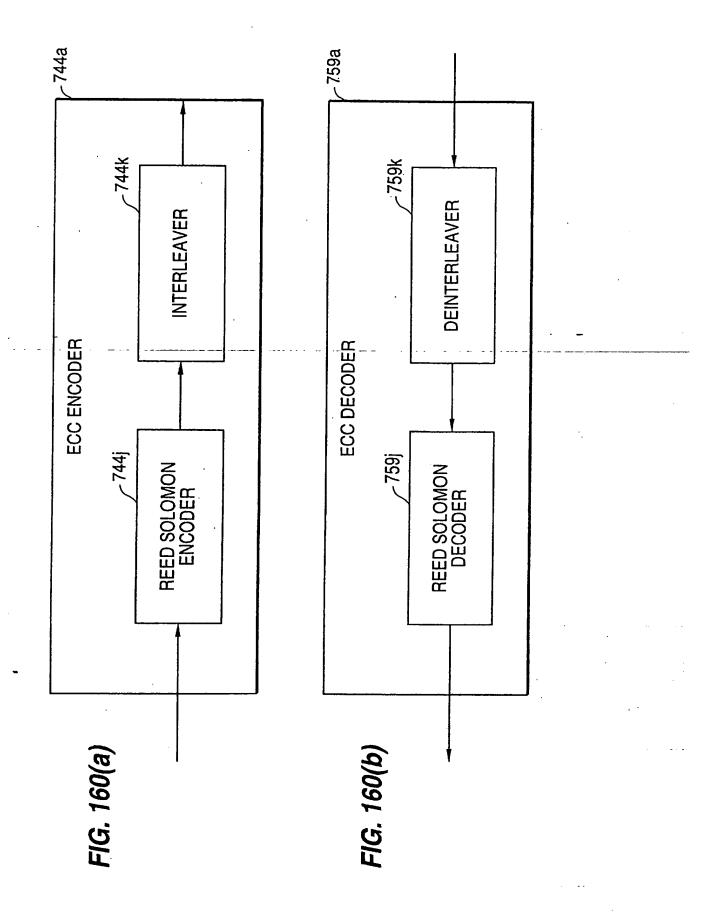


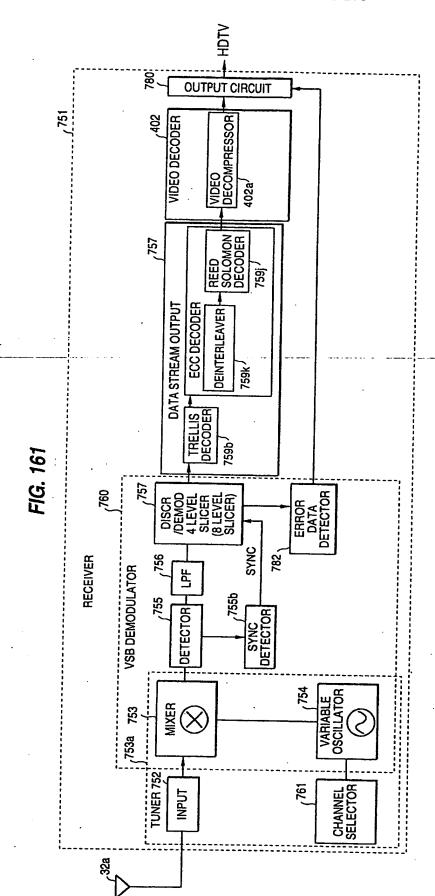
Feb. 4, 1997



, TRANSMITTED SIGNAL 품 TRANSMITTING CIRCUIT UP CONVERTER DOWN INPUT 852a DEMODULATOR MODULATOR CCDM MODULATOR C-CDM DEMODULATOR PSK ASK PSK ASA IST DATA STREAM OUTPUT **1ST DATA STREAM INPUT** FIG. 158 TRANSMITTER 743 **OUTPUT SECTION** NPUT SECTION 758 RECEIVER ECC 743a 46 1ST VIDEO ENCODER 1ST VIDEO DECODER VIDEO ENCODER VIDEO DECODER (HDTV) SIGNAL







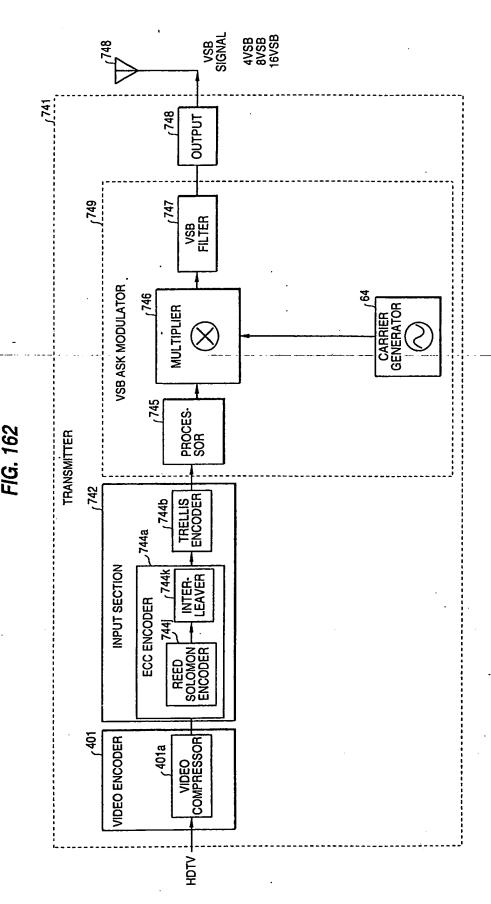


FIG. 163

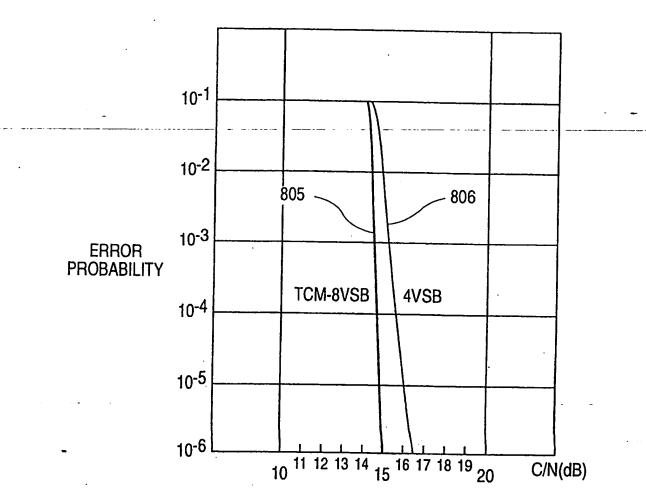
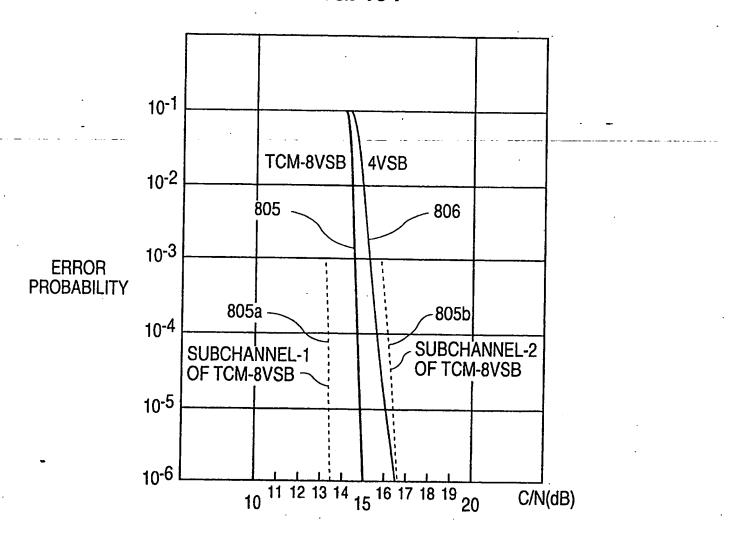


FIG. 164



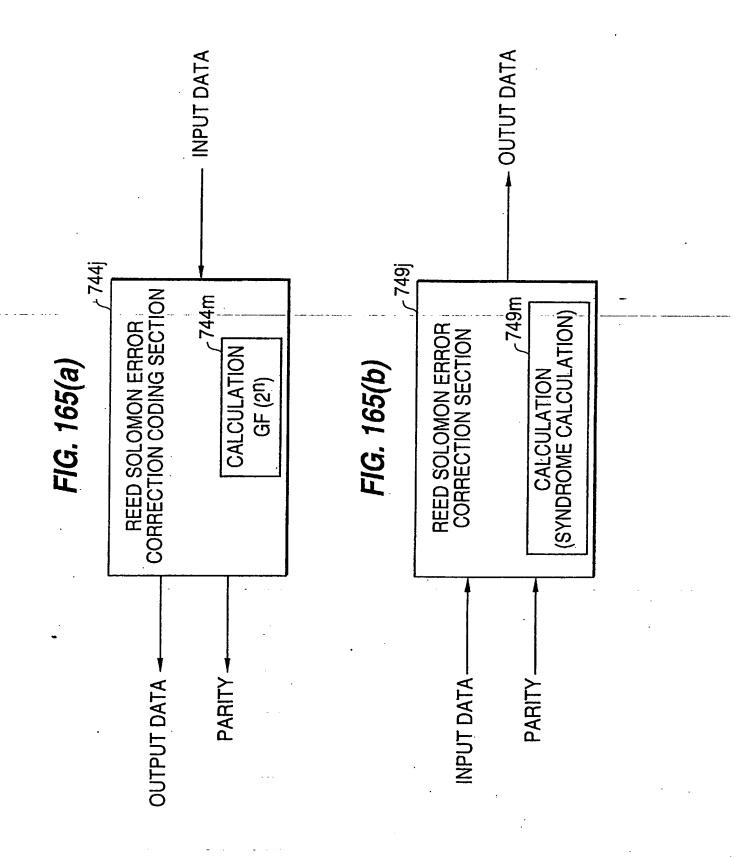
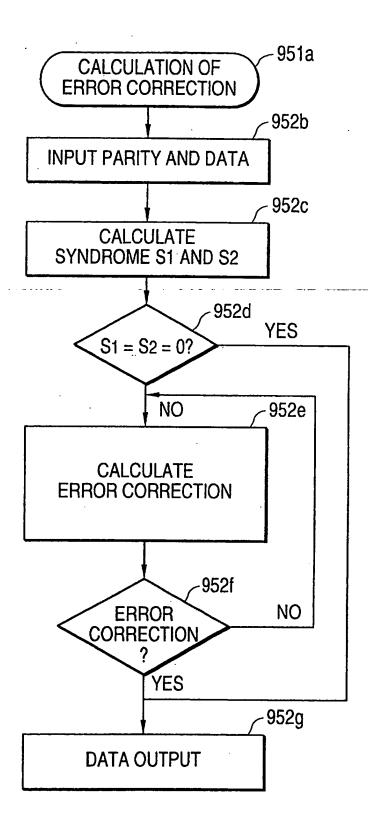
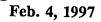
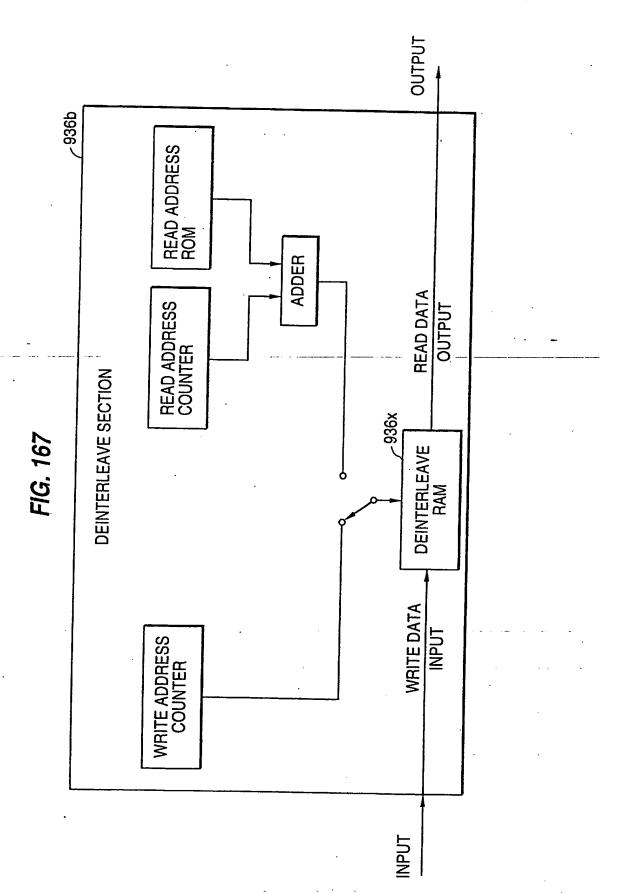
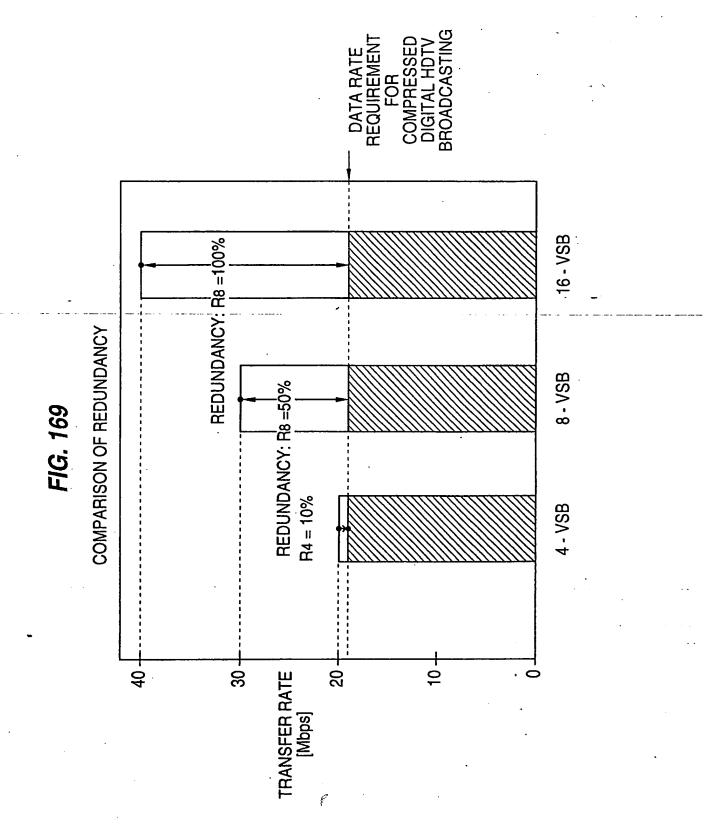


FIG. 166









TRANSMITTED SIGNAL 품 RECEIVED SIGNAL INPUT CIRCUIT , 24a TRANSMITTING CIRCUIT , 5a 24 CONVERTER DOWN CONVERTER 852a 852b 760 MODULATOR MODULATOR demodulator modulator 4VSB 8VSB 16VSB 4VSB 8VSB 16VSB 742 757 -758c TDM M D M DATA STREAM INPUT DATA STREAM INPUT **OUTPUT SECTION** INPUT SECTION **TRANSMITTER** 743a 758a ECC ENCODER HIGH GAIN ECC ENCODER LOW GAIN ECC DECODER HIGH GAIN ECC DECODER LOW GAIN RECEIVER 743b 758b LOW PRIORITY HIGH PRIORITY PRIORITY PRIORITY HGH <u></u>8 1ST VIDEO DECODER HIGH PRIORITY (ADDRESS, SYNC) - 401a VIDEO ENCODER 1ST VIDEO ENCODER HIGH PRIORITY VIDEO DECODER 7 402a 2ND VIDEO DECODER LOW PRIORITY 401d ~402d VIDEO ENCODER VIDEO DECODER **LOW PRIORITY** HDTV SIGNAL OR SDTV X n HDTV OR LOW GRADE HDTV OR SDTV X n

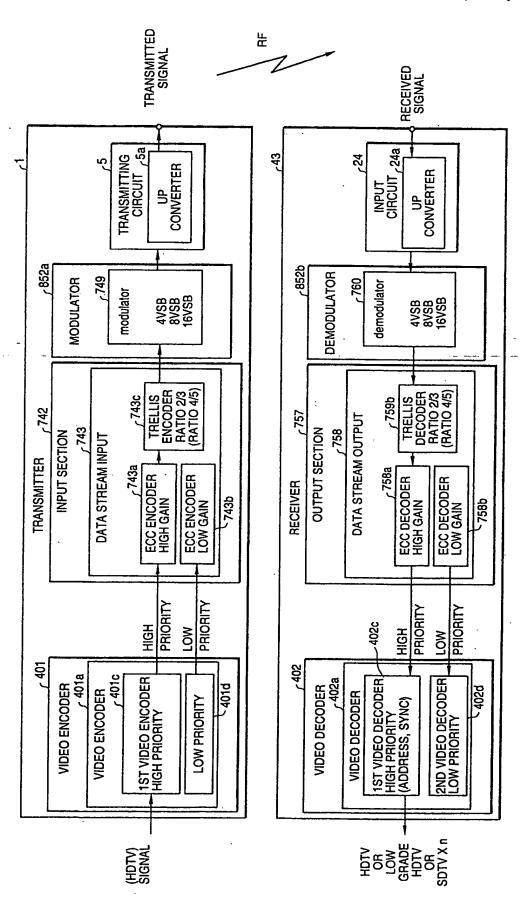
FIG. 170

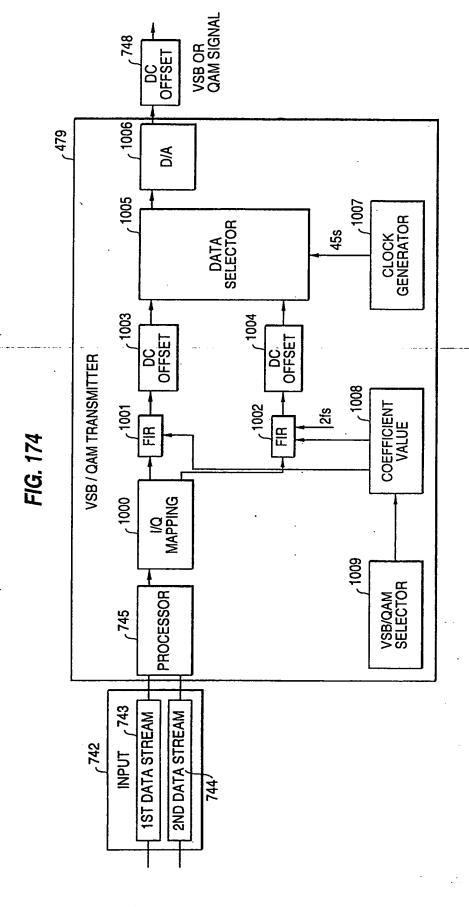
R

TRANSMITTING SIGNAL RECEIVED SIGNAL TRANSMITTING CIRCUIT 5a UP CONVERTER DOWN CONVERTER INPUT CIRCUIT 852a ₇852b **DEMODULATOR** 749 760 MODULATOR demodulator modulator 8VSB (32QAM) 8VSB (32QAM) 20 **TRANSMITTER** RECEIVER DATA STREAM INPUT, 744b OUTPUT SECTION 759 TRELLIS ENCODER RATIO 2/3 (RATIO 4/5) DATA STREAM OUTPUT, 759b TRELLIS DECODER RATIO 2/3 (RATIO 4/5) 742 757 INPUT SECTION 744a ECC ENCODER 759a ECC DECODER 7 401a 7 402a 7 401 7 402 VIDEO ENCODER VIDEO ENCODER VIDEO DECODER VIDEO DECODER HDTV SIGNAL

FIG. 171

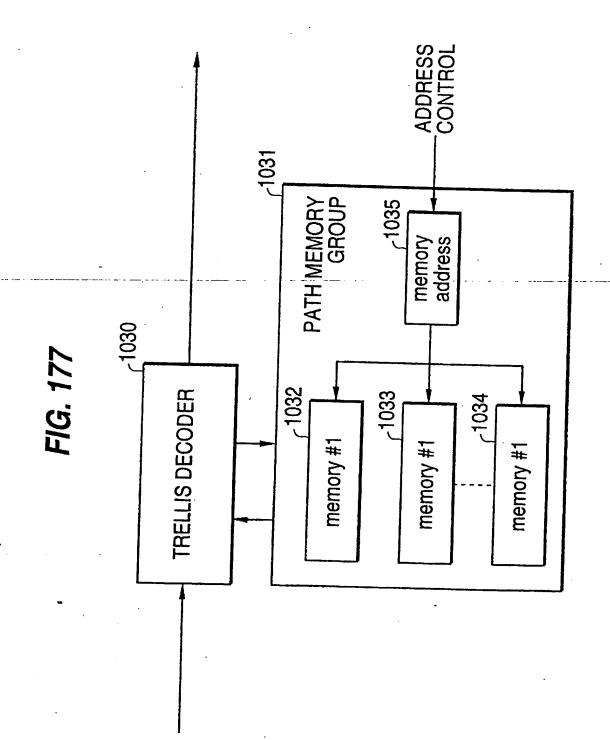
FIG. 172

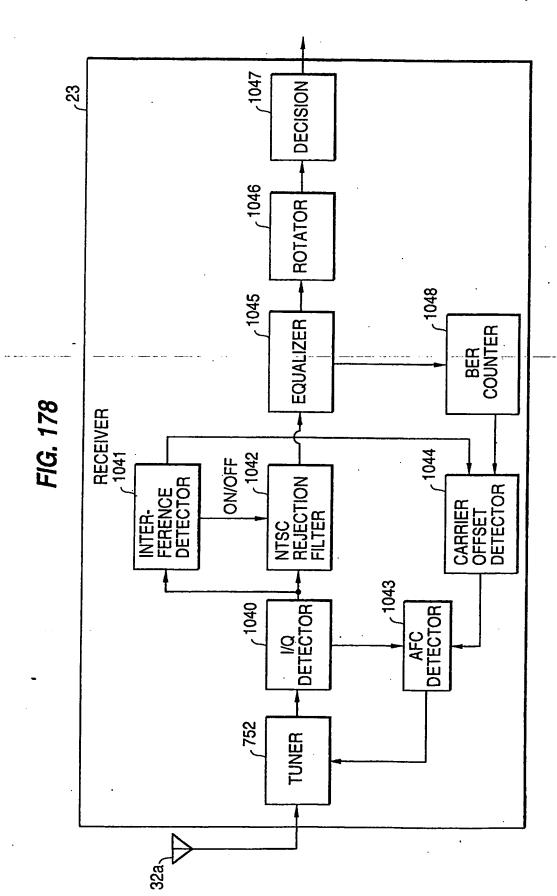


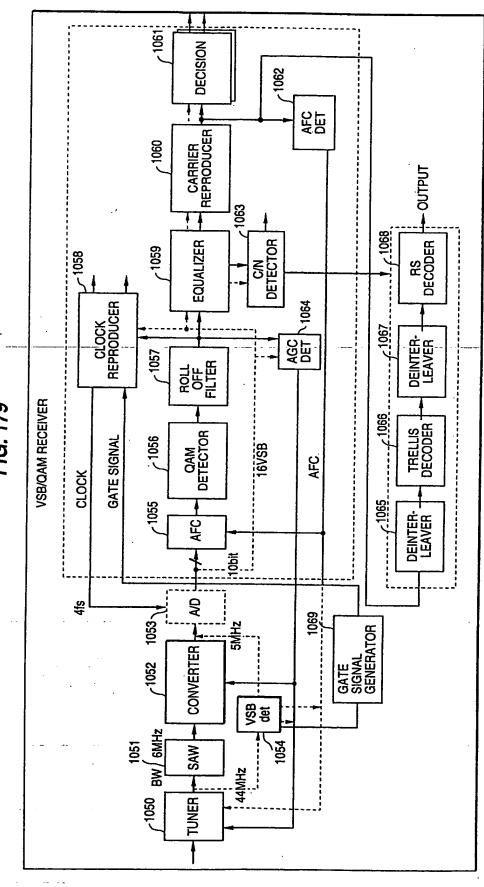


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iG. 179